ANALOG COMMUNICATION LAB

LABORATORY MANUAL

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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGG

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY
(Sponsored by CMR Educational Society)
(Affiliated to JNTU, Hyderabad)
Secunderabad-14.

VISION

To evolve into a center of excellence in Engineering Technology through creative and innovative practices in teaching-learning, promoting academic achievement & research excellence to produce internationally accepted competitive and world class professionals.

MISSION

To provide high quality academic programmes, training activities, research facilities and opportunities supported by continuous industry institute interaction aimed at employability, entrepreneurship, leadership and research aptitude among students.

QUALITY POLICY

- Impart up-to-date knowledge to the students in Electronics & Communication area to make them quality engineers.
- Make the students experience the applications on quality equipment and tools.
- Provide systems, resources and training opportunities to achieve continuous improvement.
- Maintain global standards in education, training and services.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: PROFESSIONALISM & CITIZENSHIP To create and sustain a community of learning in which students acquire knowledge and learn to apply it professionally with due consideration for ethical, ecological and economic issues.
PEO2: TECHNICAL ACCOMPLISHMENTS To provide knowledge based services to satisfy the needs of society and the industry by providing hands on experience in various technologies in core field.
PEO3: INVENTION, INNOVATION AND CREATIVITY To make the students to design, experiment, analyze, interpret in the core field with the help of other multi disciplinary concepts wherever applicable.
PEO4: PROFESSIONAL DEVELOPMENT To educate the students to disseminate research findings with good soft skills and become a successful entrepreneur.
PEO5: HUMAN RESOURCE DEVELOPMENT To graduate the students in building national capabilities in technology, education and research.

CODE OF CONDUCT FOR THE LABORATORIES

- **All students must observe the Dress Code while in the laboratory.**
- **Sandals or open-toed shoes are NOT allowed.**
- **Foods, drinks and smoking are NOT allowed.**
- **All bags must be left at the indicated place.**
- **The lab timetable must be strictly followed.**
- **Be PUNCTUAL for your laboratory session.**
- **Program must be executed within the given time.**
- **Noise must be kept to a minimum.**
- **Workspace must be kept clean and tidy at all time.**
- **Handle the systems and interfacing kits with care.**
- **All students are liable for any damage to the accessories due to their own negligence.**
- **All interfacing kits connecting cables must be RETURNED if you taken from the lab supervisor.**
- **Students are strictly PROHIBITED from taking out any items from the laboratory.**
- **Students are NOT allowed to work alone in the laboratory without the Lab Supervisor**
- **USB Ports have been disabled if you want to use USB drive consult lab supervisor.**
- **Report immediately to the Lab Supervisor if any malfunction of the accessories, is there.**

Before leaving the lab

- **Place the chairs properly.**
- **Turn off the system properly**
- **Turn off the monitor.**
- **Please check the laboratory notice board regularly for updates.**

CONTENTS

EXPERIMENT NO-1 DATE:

AMPLITUDE MODULATION &DEMODULATION

AIM: To study the function of Amplitude Modulation & Demodulation (under modulation, perfect modulation & over modulation) and also to calculate the modulation index.

APPARATUS :

1. Amplitude Modulation & De modulation trainer kit.
2. C.R.O (20MHz)
3. Function generator (1MHz).
4. Connecting cords & probes.
5. PC with windows(95/98/XP/NT/2000)
6. MATLAB Software with communication toolbox

THEORY:

Modulation is defined as the process of changing the characteristics (Amplitude, Frequency or Phase) of the carrier signal (high frequency signal) in accordance with the intensity of the message signal (modulating signal).

Amplitude modulation is defined as a system of modulation in which the amplitude of the carrier is varied in accordance with amplitude of the message signal (modulating signal).

The message signal is given by the expression.

$Em(t) = Em \cos Wmt$

Where Wm is -----> Angular frequency

Em --------→ Amplitude

Carrier voltage $Ec(t) = Ec \cos Wct$

$E(t) = Ec + KaEm \cos Wmt$

$KaEm \cos Wmt$ -----→ change in carrier amplitude

Ka-----→ constant

The amplitude modulated voltage is given by

$E = E(t) \cos Wct$

From above two equations

E= (Ec+KaEm cosWmt) cosWct.

E= (1+KaEm/Ec cosWmt) Ec cosWct

E= Ec(1+Ma cosWmt)cosWct

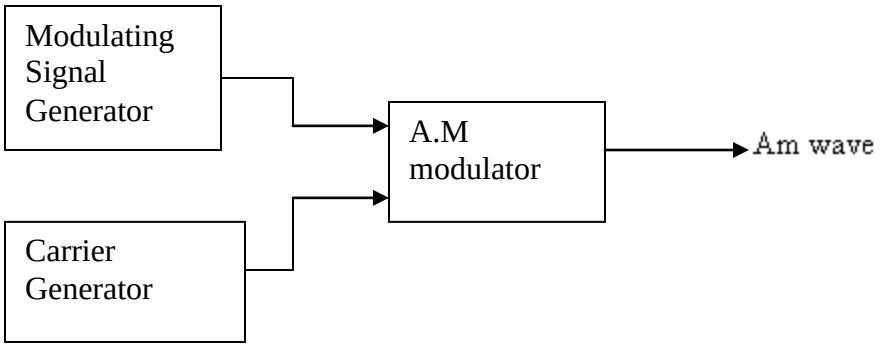
Where Ma-----→ depth of modulation/ modulation index/modulation factor

Ma=KaEm/Ec

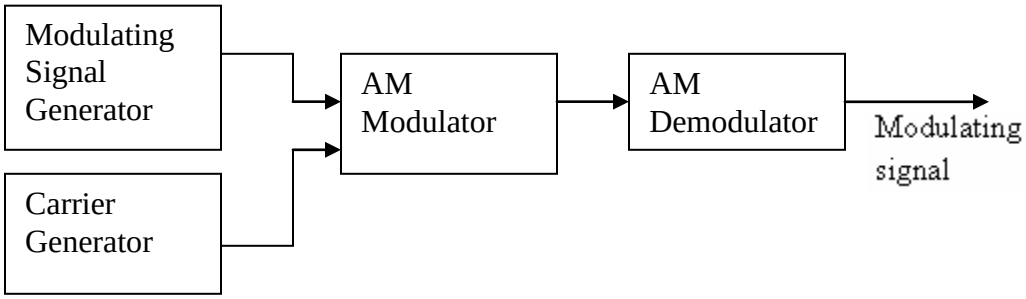
100* Ma gives the percentage of modulation.

BLOCK DIAGRAM:

Modulation



Demodulation



PROGRAM:

% program for AM modulation and demodulation

close all

clear all

```
clc
fs=8000;
fm=20;
fc=500;
Am=1;
Ac=1;
t=[0:0.1*fs]/fs;
m=Am*cos(2*pi*fm*t);
c=Ac*cos(2*pi*fc*t);
ka=0.5;
u=ka*Am;
s1=Ac*(1+u*cos(2*pi*fm*t)).*cos(2*pi*fc*t);
subplot(4,3,1:3);
plot(t,m);
title('Modulating or Message signal(fm=20Hz)');
subplot(4,3,4:6);
plot(t,c);
title('Carrier signal(fc=500Hz)');
subplot(4,3,7);
plot(t,s1);
title('Under Modulated signal(ka.Am=0.5)');
Am=2;
ka=0.5;
u=ka*Am;
s2=Ac*(1+u*cos(2*pi*fm*t)).*cos(2*pi*fc*t);
subplot(4,3,8);
plot(t,s2);
title('Exact Modulated signal(ka.Am=1)');
Am=5;
ka=0.5;
u=ka*Am;
```

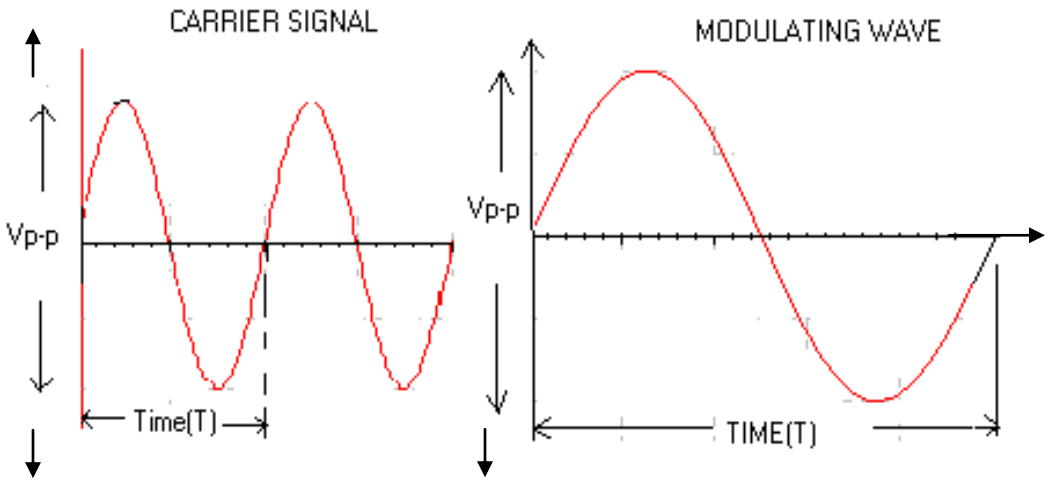
```
s3=Ac*(1+u*cos(2*pi*fm*t)).*cos(2*pi*fc*t);
subplot(4,3,9);
plot(t,s3);
title('Over Modulated signal(ka.Am=2.5)');
r1= s1.*c;
[b a] = butter(1,0.01);
mr1= filter(b,a,r1);
subplot(4,3,10);
plot(t,mr1);
title(' deModulated signal for(ka.Am=0.5)');
r2= s2.*c;
[b a] = butter(1,0.01);
mr2= filter(b,a,r2);
subplot(4,3,11);
plot(t,mr2);
title(' deModulated signal for(ka.Am=1)');
r3= s3.*c;
[b a] = butter(1,0.01);
mr3= filter(b,a,r3);
subplot(4,3,12);
plot(t,mr3);
title(' deModulated signal for(ka.Am=2.5)');
```

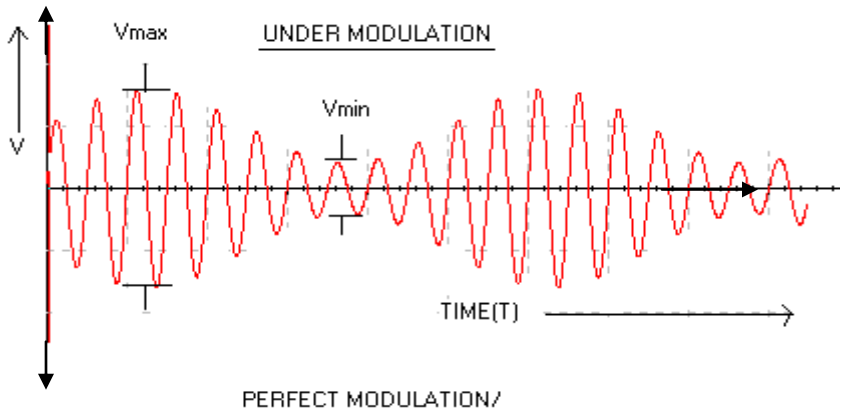
PROCEDURE:-

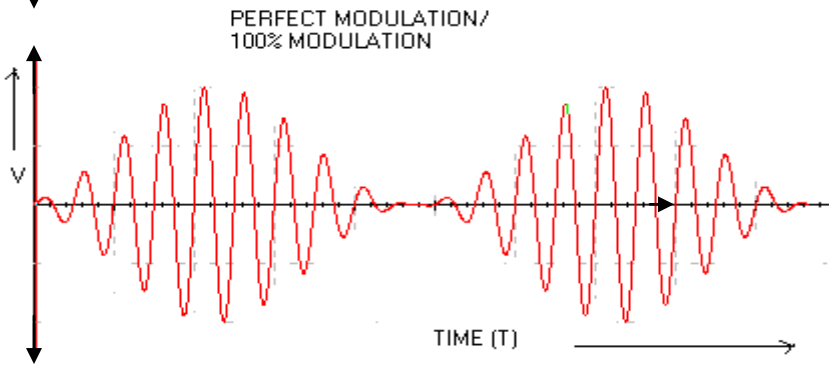
1. Connect the AC Adapter to the mains and the other side to the Experimental Trainer. Switch ‘ON’ the power.
2. Observe the carrier and modulating waveforms and note their frequencies. (Carrier frequency is around 100 KHz and amplitude is variable from 0 -8Vp-p, modulating signal is 1KHz).
3. Connect the carrier and modulating signals to the modulator circuit.
4. Observe the amplitude modulated wave.

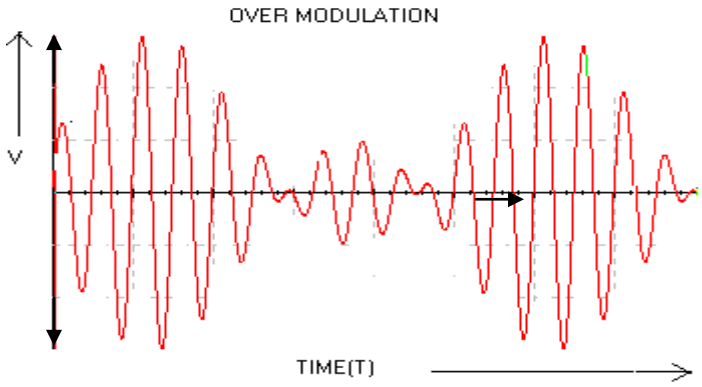
5. Connect Carrier I/P to ground and apply a 2V peak to peak AF Signal input to (modulating I/P) and adjust P1 in anti-clock wise position to get minimum A.C output.
6. Connect modulating I/P to ground and apply a 3V peak to peak carrier signal to carrier I/P and adjust P2 in clock wise direction to get minimum A.C ouyput..
7. Connect modulating input &carrier input to ground and adjust P3 for zero D.C output.
8. Make modulating i/p 2 Vpp and carrier i/p 3 Vpp peak to peak and adjust potentiometer P4 for maximum output.
9. Calculate maximum and minimum points on the modulated envelope on a CRO and calculate the depth of modulation.
10. Observe that by varying the modulating voltage, the depth of modulation varies.
11. During demodulation connect this AM output to the input of the demodulator.
12. By adjusting the RC time constant (i.e., cut off frequency) of the filter circuit we get minimum distorted output.
13. Observe that this demodulated output is amplified has some phase delay because of RC components.
14. Also observe the effects by changing the carrier amplitudes.
15. In all cases, calculate the modulation index.

EXPECTED WAVEFORMS:-

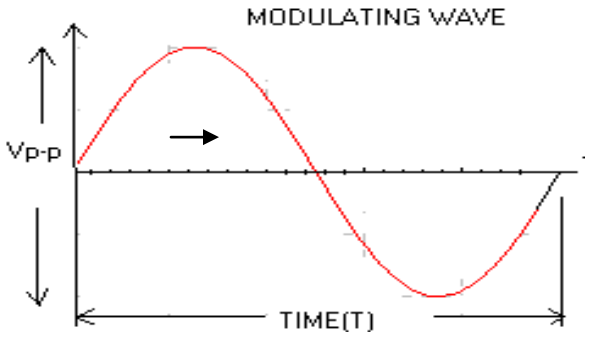








Demodulated signal



OBSERVATIONS:

Modulation

	Vc (V)	Vm (V)	Vmax (V)	Vmin (V)	m=(Vmax-Vmin)/ (Vmax+Vmin)	m= Vm/Vc
Under modulation						
Perfect modulation						
Over modulation						

Demodulation

Modulating signal Frequency	Demodulated output signal frequency

RESULT:

QUESTIONS

1. Define AM and draw its spectrum?
2. Draw the phase's representation of an amplitude modulated wave?
3. Give the significance of modulation index?
4. What are the different degrees of modulation?
5. What are the limitations of square law modulator?
6. Compare linear and nonlinear modulators?
7. Compare base modulation and emitter modulation?
8. Explain how AM wave is detected?
9. Define detection process?
10. What are the different types of distortions that occur in an envelop detector? How can they be eliminated?
11. What is the condition of for over modulation?

12. Define modulation & demodulation?
13. What are the different types of linear modulation techniques?
14. Explain the working of carrier wave generator.
15. Explain the working of modulator circuit.

EXPERIMENT NO-2 DATE:

DSB-SC MODULATOR & DETECTOR

AIM: To study the working of the Balanced Modulator and demodulator.

APPARATUS:

1. Balanced modulator trainer kit
2. C.R.O (20MHz)
3. Connecting cords and probes
4. Function generator (1MHz)
5. PC with windows (95/98/XP/NT/2000)
6. MATLAB Software with communication toolbox

THEORY:

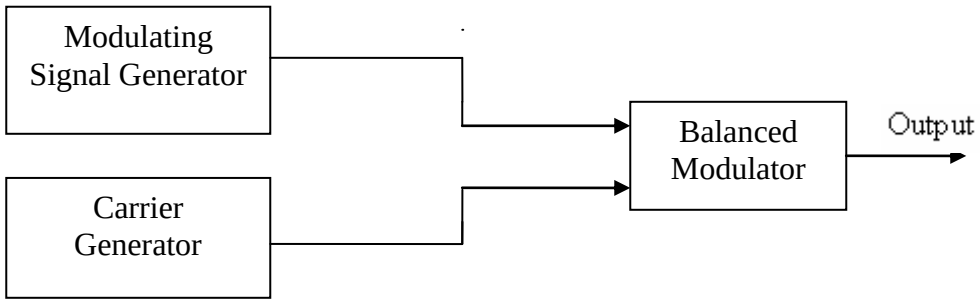
Balanced modulator circuit is used to generate only the two side bands DSB-SC. The balanced modulation system is a system is a system of adding message to carrier wave frequency there by only the side bands are produced. It consists of two AM modulators arranged in a balanced configuration. The AM modulator is assumed to be identical. The carrier input to the two modulators is same.

If we eliminate or suppress the carrier then the system becomes suppressed carrier DSB-SC. In this we need reinsert the carrier is complicated and costly. Hence the suppressed carrier DSB system may be used in point to point communication system.

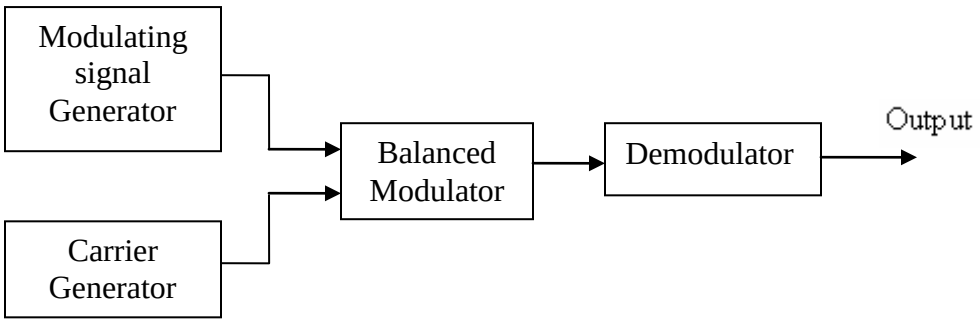
Generation of suppressed carrier amplitude modulated volt balanced modulator may be of the following types.

1. Using transistors or FET.
2. Using Diodes

BLOCK DIAGRAM: Modulation



Demodulation



PROGRAM:

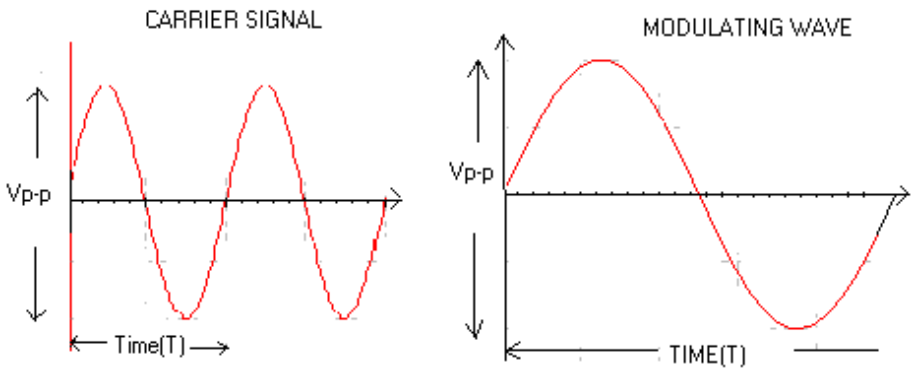
```
% program for dsbsc modulation and demodulation
close all
clear all
clc
t =0:0.000001:.001;
Vm= 1;
Vc= 1;
fm = 2000;
fc= 50000;
m_t = Vm*sin(2*pi*fm*t);
subplot(4,1,1);
plot(t,m_t);
c_t = Vc*sin(2*pi*fc*t);
subplot(4,1,2);
plot(t,c_t);
subplot(4,1,3);
s_t = m_t.*c_t;
hold on;
plot(t,s_t);
plot(t,m_t,'r:');
plot(t,-m_t,'r:');
hold off;
```

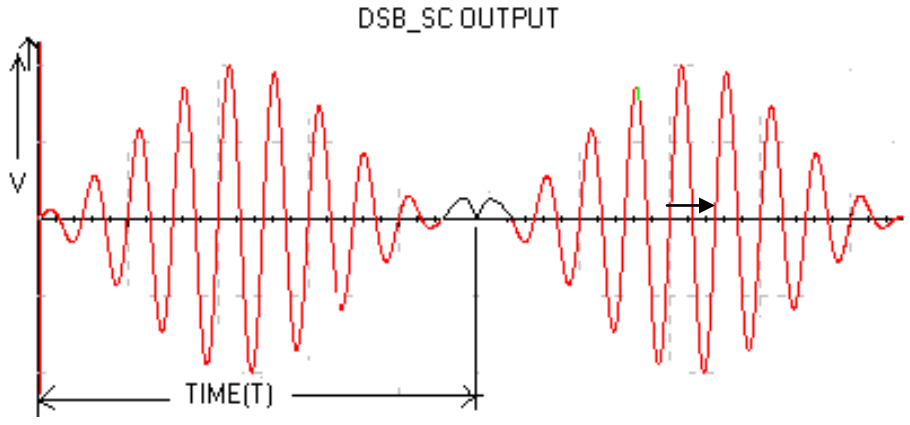
```
r = s_t.*c_t;
[b a] = butter(1,0.01);
mr= filter(b,a,r);
subplot(4,1,4);
plot(t,mr);
```

PROCEDURE:-

1. Connect the circuit as per the given circuit diagram.
2. Switch on the power to the trainer kit.
3. Apply a 100KHz, 0.1 peak sinusoidal to the carrier input and a 5KHz, 0.1 peak sinusoidal to the modulation input.
4. Measure the output signal frequency and amplitude by connecting the output to CRO.
5. And note down the output signals.

EXPECTED WAVEFORMS:-





OBSERVATIONS:

Carrier Signal		Message signal		Modulated signal output		Demodulated Signal output	
Fc(Hz)	Vc(volts)	Fm(Hz)	Vm(v)	Fo(Hz)	Vo(v)	F(Hz)	V(v)

RESULT:

QUESTIONS

1. What are the two ways of generating DSB_SC?
2. What are the applications of balanced modulator?
3. What are the advantages of suppressing the carrier?
4. What are the advantages of balanced modulator?
5. What are the advantages of Ring modulator?
6. Write the expression for the output voltage of a balanced modulator?
7. Explain the working of balanced modulator and Ring Modulator using diodes.

EXPERIMENT.NO-3 DATE:

SSB-SC MODULATOR & DETECTOR

(PHASE SHIFT METHOD)

AIM:- To generate SSB using phase method and detection of SSB signal using Synchronous detector.

APPARATUS:-

1. SSB trainer kit
2. C.R.O (20MHz)
3. Patch cards
4. CRO probes

THEORY:

AM and DSBSC modulation are wasteful of band width because they both require a transmission bandwidth which is equal to twice the message bandwidth In SSB only one side band and the carrier is used. The other side band is suppressed at the transmitter, but no information is lost. Thus the communication channel needs to provide the same band width, when only one side band is transmitted. So the modulation system is referred to as SSB system.

The base band signal may not be recovered from a SSB signal by the Use of a diode modulator. The bae band signal can be recovered if the spectral component of the output i.e either the LSB or USB is multiplied by the carrier signal.

Consider the modulating signal

$$M(t)=A_m \cos W_{mt}$$

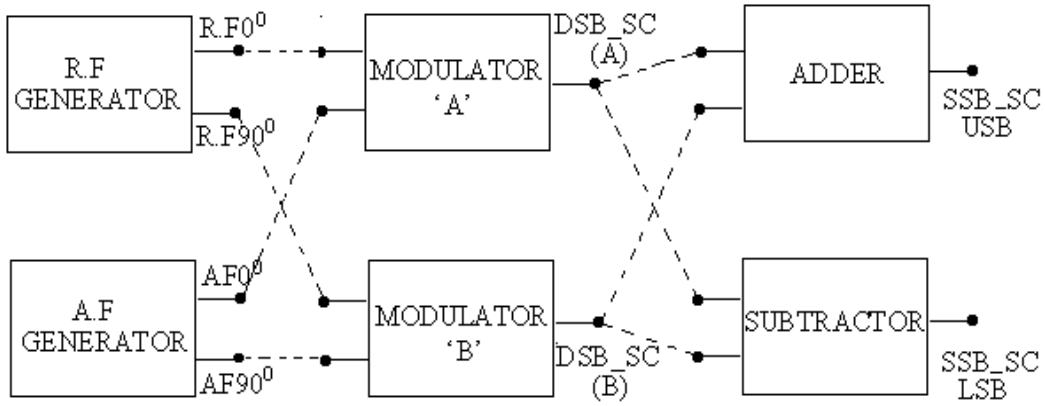
$$C(t)=A_c \cos W_{ct}$$

$$M(t)c(t)= A_cA_m \cos W_{mt} \cos W_{ct}$$

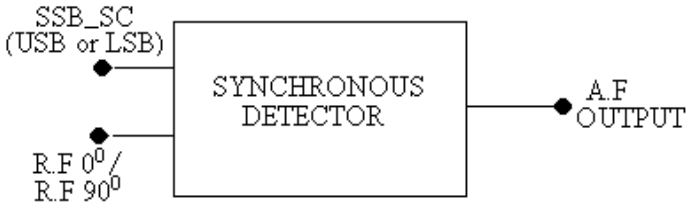
The above signal when passed through a filter, only one of the above component is obtained which lays the SSB signal.

BLOCK DIAGRAM: -

SSB MODULATION



SSB DEMODULATION/SYNCHRONOUS DETECTOR



PROGRAM:-

```
% program for ssb modulation and demodulation
close all
clear all
clc
fs=8000;
fm=20;
fc=50;
Am=1;
Ac=1;
t=[0:0.1*fs]/fs;
subplot(5,1,1);
m1=Am*cos(2*pi*fm*t);
plot(t,m1);
title('Message Signal');
```

```
m2=Am*sin(2*pi*fm*t);
subplot(5,1,2)
c1=Ac*cos(2*pi*fc*t);
plot(t,c1)
title('Carrier Signal');
c2=Ac*sin(2*pi*fc*t);
subplot(5,1,3)
% Susb=0.5* Am*cos(2*pi*fm*t).* Ac*cos(2*pi*fc*t) -- 0.5* Am*sin(2*pi*fm*t).*
Ac*sin(2*pi*fc*t);
Susb=0.5*m1.*c1-0.5*m2.*c2;
plot(t,Susb);
title('SSB-SC Signal with USB');
subplot(5,1,4);
Slsb=0.5*m1.*c1+0.5*m2.*c2;
plot(t,Slsb);
title('SSB-SC Signal with LSB');
r = Susb.*c1;
subplot(5,1,5);
[b a] = butter(1,0.0001);
mr= filter(b,a,r);
plot(t,mr);
title('demodulated output');
```

PROCEDURE:-

SSB MODULATION

1. Connect the Adaptor to the mains and the other side to the Experimental Trainer Switch 'ON' the power.
2. (a) Connect carrier f_c 90^0 to A_{in} of Balanced Modulator –A and adjust its amplitude to 0.1Vpp.

(b). Connect modulating signal f_m 0^0 5Vpp to B_{in} of the Balanced Modulator-A.

3. Observe the DSB-A output on CRO.

4. Connect fc 0^0 at 0.1 Vpp at C_{in} of Balanced Modulator B. Connect fm 90^0 at 5 Vpp at D_{in} of Balanced Modulator B.

5. Connect the DSB-A output and DSB-B output to the summing amplifier. Observe the output (SSB output) on the spectrum analyzer. This gives single side band (upper) only while the lower side band is cancelled in the summing Amplifier.

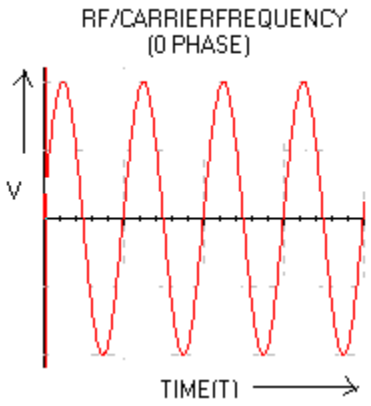
SSB DEMODULATION

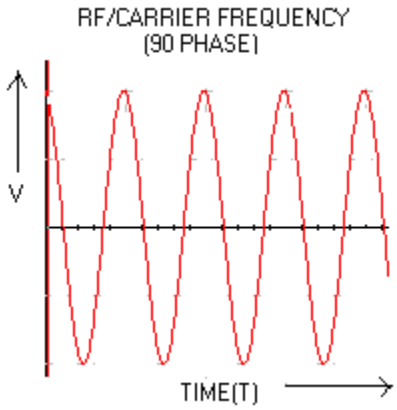
1. Connect the carrier fc 0^0 and SSB output to the synchronous detector.
2. Connect the demodulator output on the oscilloscope which is the recovered modulating signal.

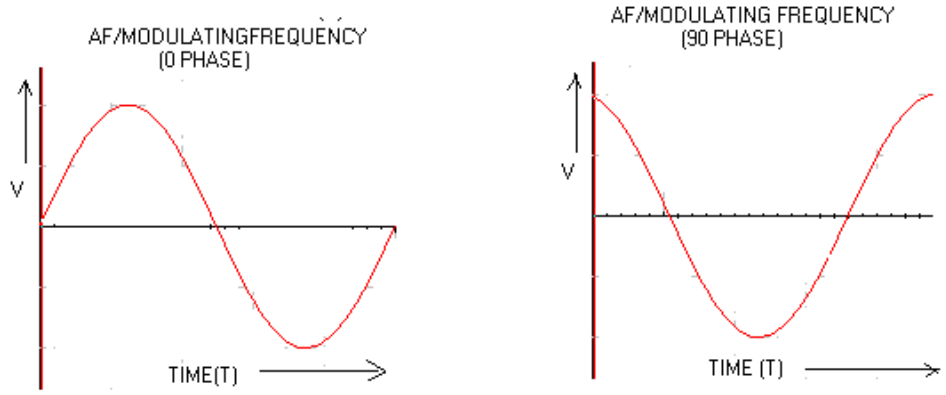
OBSERVATIONS:

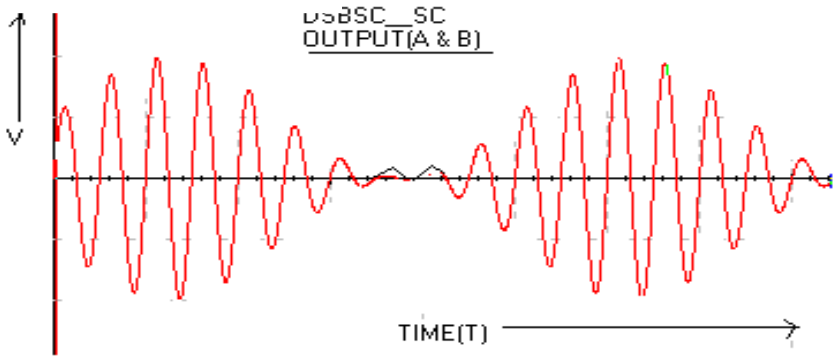
Carrier signal		Modulating signal		Balanced modulator-A		Balanced modulator-B		Adder/ Subtractor Output		Synchronous detector	
Fc	Vc	Fm	Vm	Vmax	Vmin	Vmax	Vmin	Vmax	Vmin	Fd	Vd

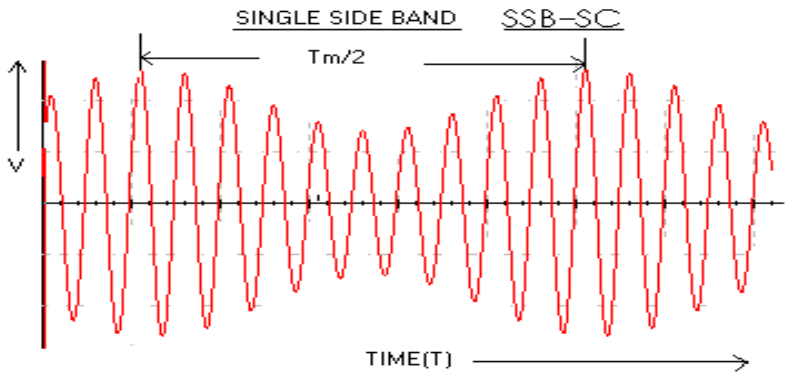
EXPECTED WAVE FORMS: -

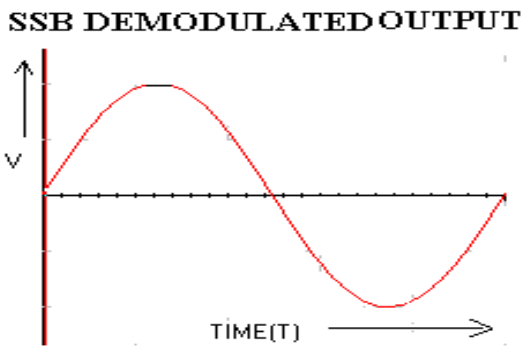





AF/MODULATINGFREQUENCY
(0 PHASE)
V
TIME(T)
AF/MODULATING FREQUENCY
(90 PHASE)
V
TIME (T)


DSBSC_SC
OUTPUT(A & B)
V
TIME(T)


SINGLE SIDE BAND
SSB-SC
Tm/2
V
TIME(T)


SSB DEMODULATED OUTPUT
V
TIME(T)

RESULT:

QUESTIONS

1. What are the different methods to generate SSB-SC signal?
2. What is the advantage of SSB-SC over DSB-SC?
3. Explain Phase Shift method for SSB generation.
4. Why SSB is not used for broadcasting?

SSB DETECTION

5. Give the circuit for synchronous detector?
6. What are the uses of synchronous or coherent detector?
7. Give the block diagram of synchronous detector?
8. Why the name synchronous detector?

EXPERMENT NO-4 DATE:

FREQUENCY MODULATION AND DEMODULATION

AIM: To study the process of frequency modulation and demodulation and calculate the depth of modulation by varying the modulating voltage.

APPARATUS :

1. FM modulation and demodulation kit
2. Dual trace CRO.
3. CRO probes
4. Patch cards.
5. PC with windows(95/98/XP/NT/2000)
6. MATLAB Software with communication toolbox

THEORY:

The modulation system in which the modulator output is of constant amplitude, in which the signal information is super imposed on the carrier through variations of the carrier frequency.

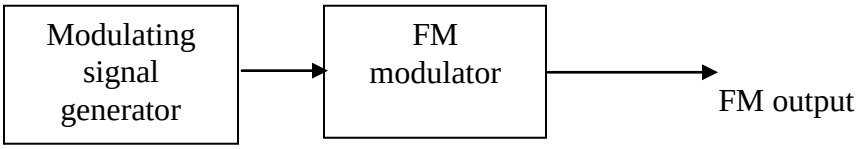
The frequency modulation is a non-linear modulation process. Each spectral component of the base band signal gives rise to one or two spectral components in the modulated signal. These components are separated from the carrier by a frequency difference equal to the frequency of base band component. Most importantly the nature of the modulators is such that the spectral components which produce decently on the carrier frquency and the base band frequencies.The spetral components in the modulated wave form depend on the amplitude.

The modulation index for FM is defined as

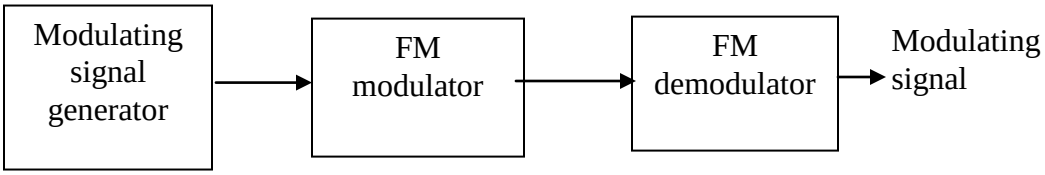
Mf= max frequency deviation/ modulating frequency.

BLOCK DIAGRAM:

Modulation



Demodulation



PROGRAM:-

```
% program for fm modulation and demodulation
close all
clear all
clc
%fm=35HZ,fc=500HZ,Am=1V,Ac=1V,B=10
fs=10000;
Ac=1;
Am=1;
fm=35;
fc=500;
B=10;
t=(0:.1*fs)/fs;
wc=2*pi*fc;
wm=2*pi*fm;
m_t=Am*cos(wm*t);
subplot(4,1,1);
plot(t,m_t);
title('Modulating or Message signal(fm=35Hz)');
c_t=Ac*cos(wc*t);
subplot(4,1,2);
plot(t,c_t);
title('Carrier signal(fm=500Hz)');
s_t=Ac*cos((wc*t)+B*sin(wm*t));
subplot(4,1,3);
```

```
plot(t,s_t);
title('Modulated signal');
d=demod(s_t,fc,fs,'fm');
subplot(4,1,4);
plot(t,d);
title('demodulated signal');
```

PROCEDURE:

1. Switch on the experimental board.
2. Observe the FM modulator output without any modulator input which is the carrier signal and note down its frequency and amplitude.
3. Connect modulating signal to FM modulator input and observe modulating signal and FM output on two channels of the CRO simultaneously.
4. Adjust the amplitude of the modulating signal until we get less distorted FM output.
5. Apply the FM output to FM demodulator and adjust the potentiometer in demodulation until we get demodulated output.

OBSERVATIONS:

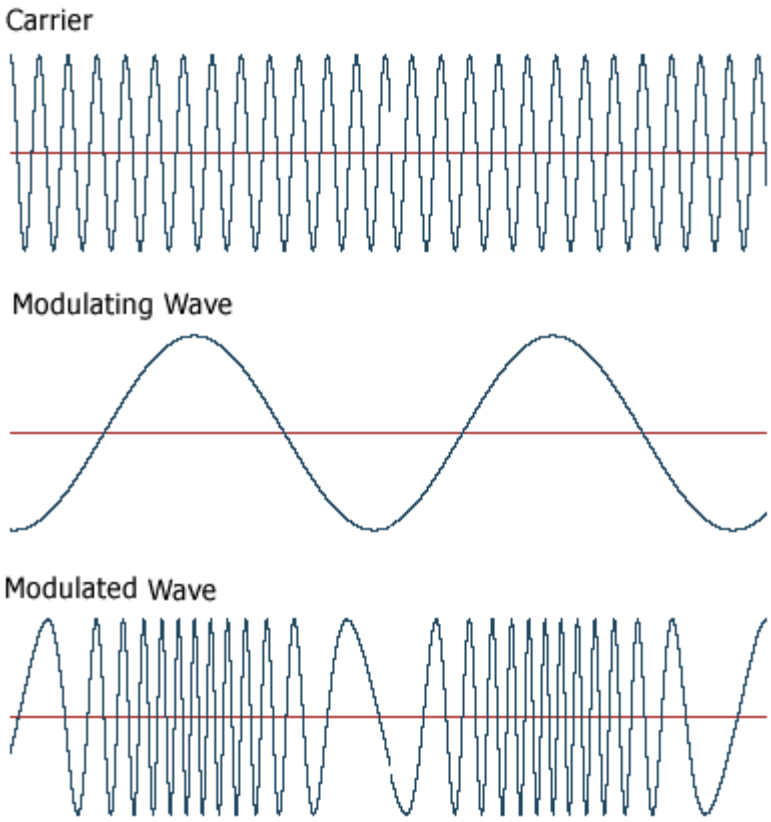
Modulation

Vm	F1	F2	Frequency deviation Fd (f1-f2)	Modulating index (f1-f2)/Fm	Band width= 2(Fd+Fm)

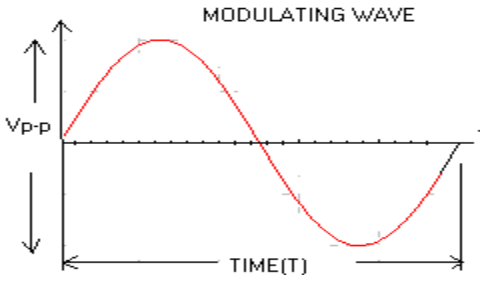
Demodulation

Modulating signal frequency	Demodulating signal frequency

EXPECTED WAVEFORMS:-



Demodulated signal



RESULT:

QUESTIONS

1. Define FM & PM.
2. What are the advantages of Angle modulation over amplitude modulation?
3. What is the relationship between PM and FM?
4. With a neat block diagram explain how PM is generated using FM.

EXPERIMENT NO-5 DATE:

STUDY OF SPECTRUM ANALYZER AND ANALYSIS OF AM AND FM SIGNALS

AIM: To verify the spectrum of AM and FM signals using spectrum analyzer.

APPARATUS / SOFTWARE REQUIRED:

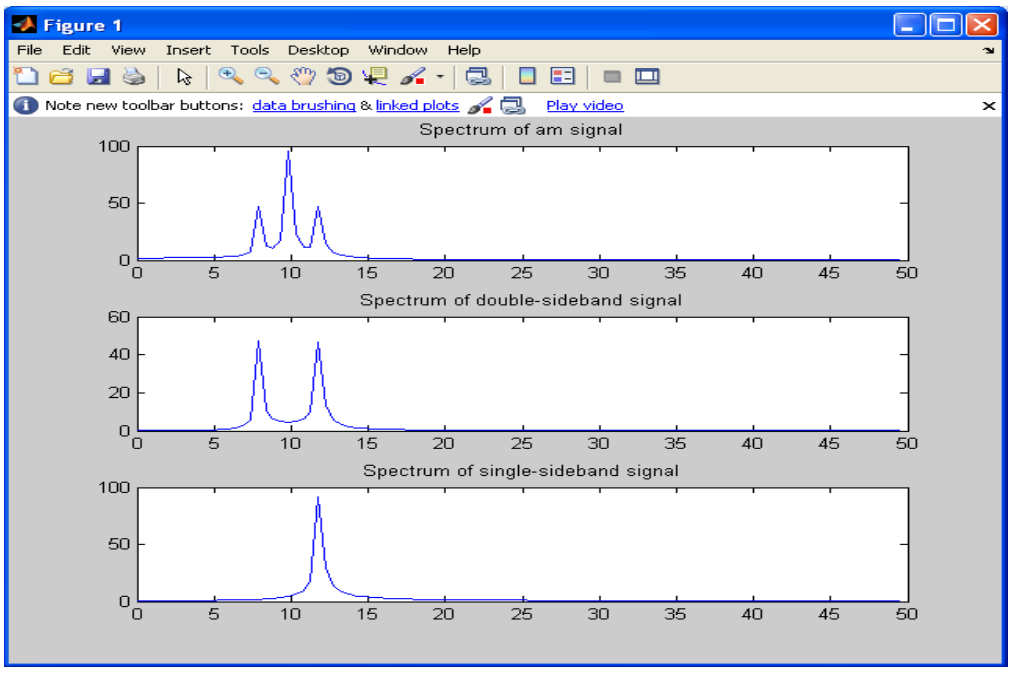
1. PC with windows(95/98/XP/NT/2000)
2. MATLAB Software with communication toolbox

PROGRAM:

```
%program of spectrum analyzer and analysis of am and fm signals
close all
clear all
clc
Fs = 100;          %sampling frq
t = [0:2*Fs+1]'/Fs;
Fc = 10;           % Carrier frequency
x = sin(2*pi*2*t);      % message signal
Ac=1;
% compute spectra of am
xam=ammod(x,Fc,Fs,0,Ac);
zam = fft(xam);
zam = abs(zam(1:length(zam)/2+1));
frqam = [0:length(zam)-1]*Fs/length(zam)/2;
% compute spectra of dsbsc
ydouble = ammod(x,Fc,Fs, 3.14,0);
zdouble = fft(ydouble);
zdouble = abs(zdouble(1:length(zdouble)/2+1));
frqdouble = [0:length(zdouble)-1]*Fs/length(zdouble)/2;
% compute spectra of ssb
ysingle = ssbmod(x,Fc,Fs,0,'upper');
zsingle = fft(ysingle);
```

```
zsingle = abs(zsingle(1:length(zsingle)/2+1));
frqsingle = [0:length(zsingle)-1]*Fs/length(zsingle)/2;
% Plot spectrums of am dsbsc and ssb
figure;
subplot(3,1,1); plot(frqam,zam);
title('Spectrum of am signal');
subplot(3,1,2); plot(frqdouble,zdouble);
title('Spectrum of double-sideband signal');
subplot(3,1,3); plot(frqsingle,zsingle);
title('Spectrum of single-sideband signal');
% spectrum of fm
xfm=fmmod(x,Fc,Fs,10);
zfm = fft(xfm);
zfm = abs(zfm(1:length(zfm)/2+1));
frqfm = [0:length(zfm)-1]*Fs/length(zfm)/2;
figure;
plot(frqfm,zfm);
title('Spectrum of fm signal');
```

EXPECTED WAVEFORMS:



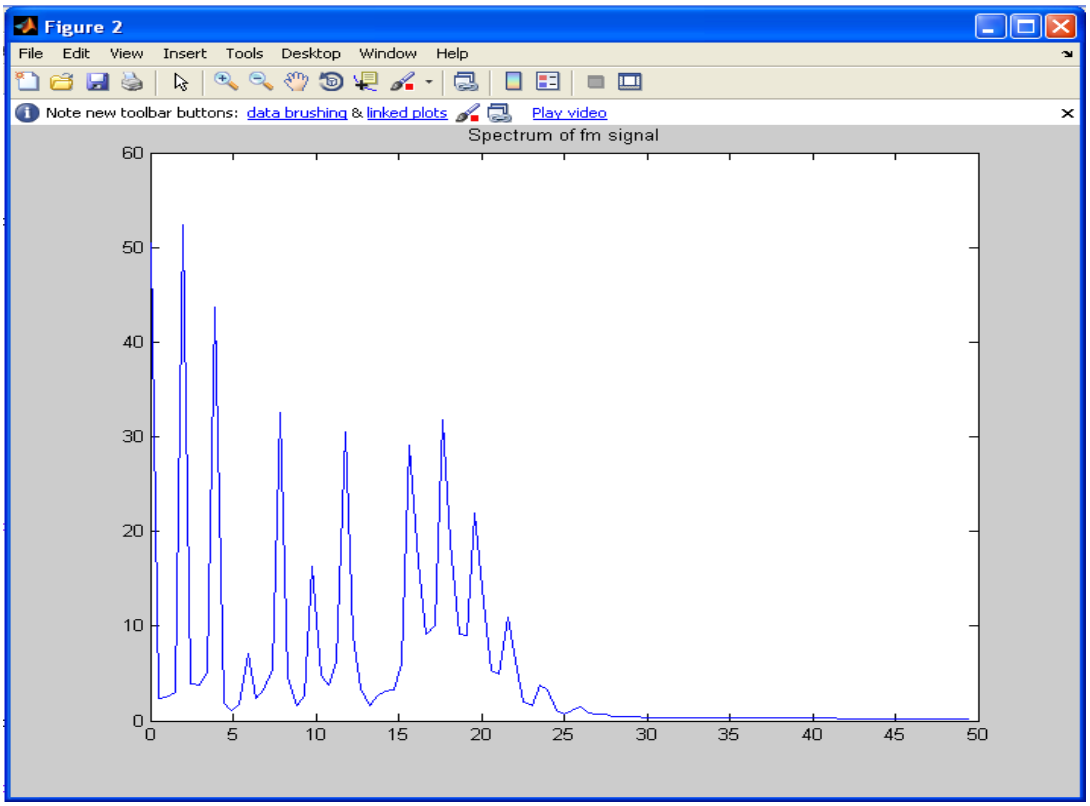


Figure 2
File Edit View Insert Tools Desktop Window Help
Note new toolbar buttons: data brushing & linked plots Play video
Spectrum of fm signal
60
50
40
30
20
10
0
0 5 10 15 20 25 30 35 40 45 50

RESULT:

EXPERIMENT.NO-6 DATE:

PRE-EMPHASIS & DE-EMPHASIS

AIM: To study the frequency response of Pre-Emphasis and De-Emphasis circuits.

APPARATUS:

1. Pre-emphasis & De-emphasis trainer kits.
2. C.R.O (20 MHz)
3. Function generator (1MHz).
4. Patch chords and Probes.
5. PC with windows (95/98/XP/NT/2000)
6. MATLAB Software with communication toolbox

THEORY:

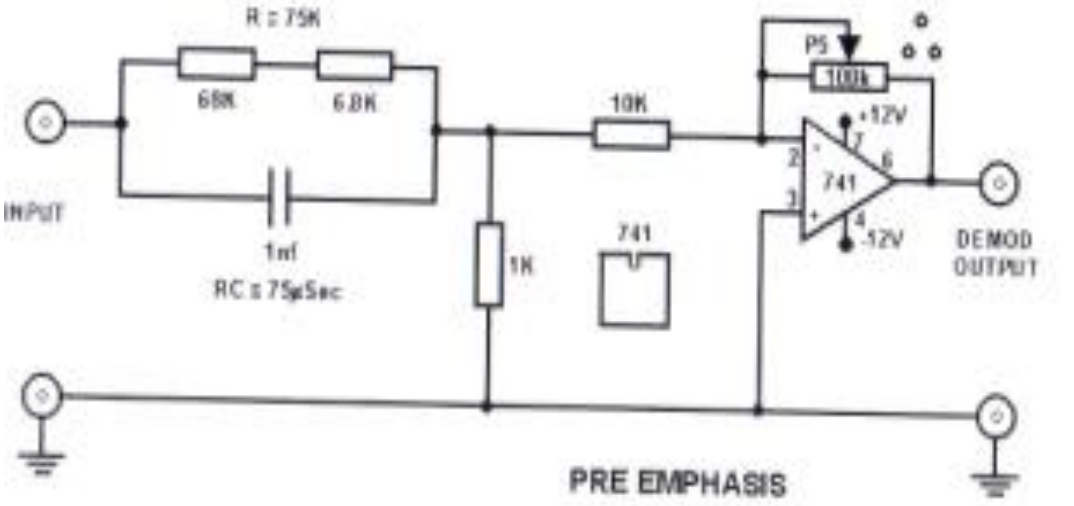
Frequency modulation is much immune to noise than amplitude modulation and significantly more immune than phase modulation. A single noise frequency will affect the output of the receiver only if it falls with in its pass band.

The noise has a greater effect on the higher modulating frequencies than on lower ones. Thus, if the higher frequencies were artificially boosted at the transmitter and correspondingly cut at the receiver, improvement in noise immunity could be expected. This booting of the higher frequencies, in accordance with a pre-arranged curve, is termed pre-emphasis, and the compensation at the receiver is called de-emphasis.

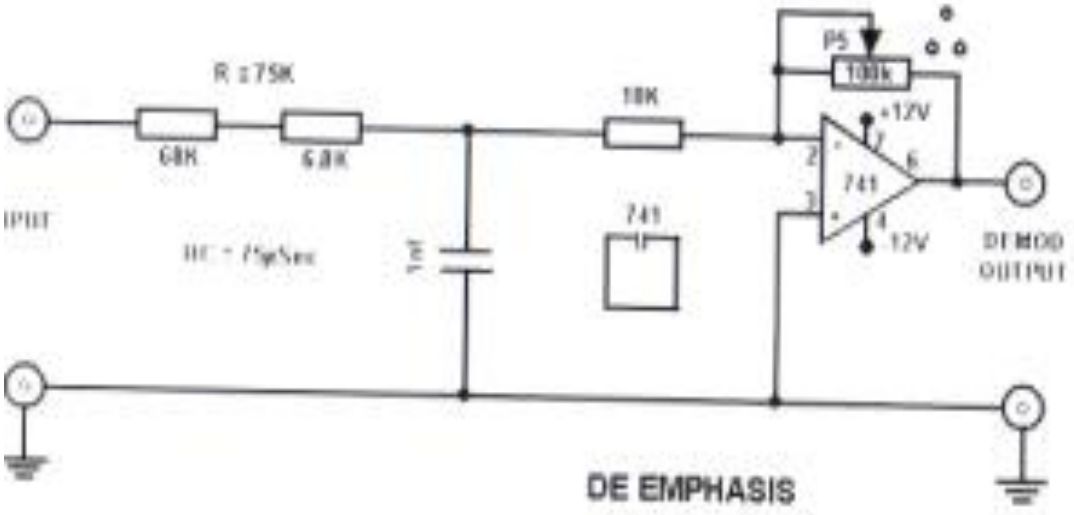
If the two modulating signals have the same initial amplitude, and one of them is pre-emphasized to (say) twice this amplitude, whereas the other is unaffected (being at a much lower frequency) then the receiver will naturally have to de-emphasize the first signal by a factor of 2, to ensure that both signals have the same amplitude in the output of the receiver. Before demodulation, I.e. while susceptible to noise interference the emphasized signal had twice the deviation it would have had without pre-emphasis, and was thus more immune to noise. Alternatively, it is seen that when this signal is de-emphasized any noise sideband voltages are de-emphasized with it, and therefore have a correspondingly lower amplitude than they would have had without emphasis again their effect on the output is reduced.

Apart from that, it would be difficult to introduce pre-emphasis and de-emphasis in existing AM services since extensive modifications would be needed, particularly in view of the huge numbers is receivers in use.

CIRCUIT DIAGRAM:



PRE EMPHASIS



DE EMPHASIS

PROGRAM:-

% program for Pre-Emphasis and De-Emphasis

close all

clear all

clc

```
num_samples = 2^13;
fs=5000;
Ts=1/fs;
fm1=20;
fm2=30;
fc=200;
t=(0:num_samples-1)*Ts;
f=(-num_samples/2:num_samples/2-1)*fs/num_samples;
mt=sin(2*pi*fm1*t);
Mf=fftshift(abs(fft(mt)));
f_cutoff_pe=15;
Wn_pe=f_cutoff_pe/(fs/2);
[b_pe,a_pe]=butter(1,Wn_pe);
[H_pe,W]=freqz(a_pe,b_pe);
a_de=b_pe;
b_de=a_pe;
[H_de,W]=freqz(a_de,b_de);
mt_pe=filter(a_pe,b_pe,mt);
Mf_pe=fftshift(abs(fft(mt_pe)));
figure(1);
subplot(211);plot(t,mt)
axis([0 .6 min(mt)-1 max(mt)+1])
grid on;title('Modulating Signal (Time Domain)')
subplot(212);plot(f,Mf)
```

```
grid on;axis([-50 50 0 max(Mf)+100])
title('Modulating Signal (Frequency Domain)')
 figure(2)
subplot(211)
semilogx(W*pi*(fs/2),abs(H_pe),'m','linewidth',2)
axis([0 fs/2 0 50])
grid on;title('Pre-emphasis Filter Magnitude Response')
subplot(212)
semilogx(W*pi*(fs/2),abs(H_de),'m','linewidth',2)
axis([0 fs/2 0 1])
grid on;title('De-emphasis Filter Magnitude Response')
figure(3)
subplot(211)
plot(t,mt_pe);
axis([0 .6 min(mt_pe)-1 max(mt_pe)+1]);
title('preemphasised signal time domain')
subplot(212);
plot(f,Mf_pe);
title('pre-emphasised signal frequency domain');
grid on;axis([-50 50 0 max(Mf_pe)+100])
```

PROCEDURE:

I-PRE-EMPHASIS

1. Connect the circuit as per the circuit diagram
2. Apply a sine wave to the input terminals of 2 V_{P-P} (Vi)

3. By varying the input frequency with fixed amplitude, note down the output amplitude (V_o) with respect to the input frequency.
4. Calculate the gain using the formula

   Gain = 20 log (V_O/ V_I) db

   Where V_O = output voltage in volts.

   V_I = Input voltage in volts.

   And plot the frequency response.

II-DE-EMPHASIS

1. Connect the circuit as per circuit diagram.
2. Repeat steps 2, 3 & 4 of Pre-Emphasis to de-emphasis also.

EXPECTED WAVEFORMS

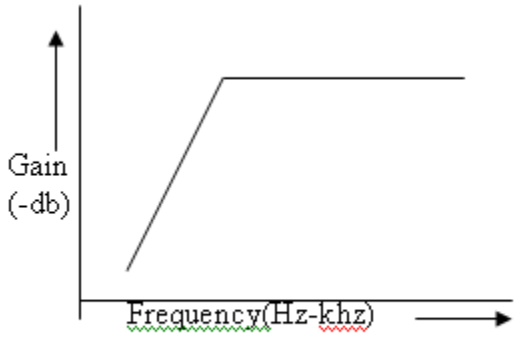


Fig: Pre-emphasis

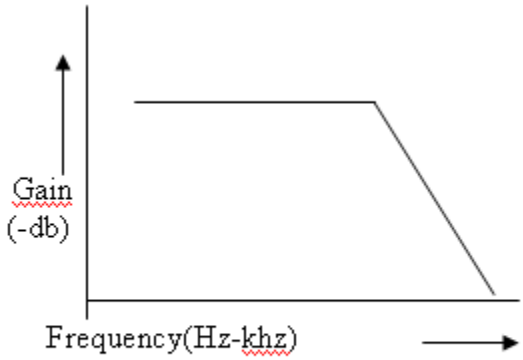


Fig: De-emphasis

TABLE:-

Pre-emphasis

Frequency(f)	Vin	Vo	Vo/Vin	Gain in db (20logVo/Vin)

De-emphasis

Frequency(f)	Vin	Vo	Vo/Vin	Gain in db (20logVo/Vin)

RESULT :

QUESTIONS

1. What is the need for pre-emphasis?
2. Explain the operation of pre-emphasis circuit?
3. Pre emphasis operation is similar to high pass filter explain how?
4. De emphasis operation is similar to low pass filter justify?
5. What is de-emphasis?
6. Draw the frequency response of a pre-emphasis circuit?
7. Draw the frequency response of a de-emphasis circuit?
8. Give the formula for the cutoff frequency of the pre-emphasis circuit?
9. What is the significance of the 3db down frequency?

EXPERIMENT NO-7 DATE:

TIME DIVISION MULTIPLEXING & DEMULTIPLEXING

AIM:

1. Study of 4 Channel Analog Multiplexing and De multiplexing Techniques.

APPARATUS:

1. TIME DIVISION MULTIPLEXING & DEMULTIPLEXING Trainer Kit.
2. C.R.O (30 MHz)
3. Patch chords.
4. PC with windows (95/98/XP/NT/2000)
5. MATLAB Software with communication toolbox

THEORY:-

The TDM is used for transmitting several analog message signals over a communication channel by dividing the time frame into slots, one slot for each message signal. The four input signals, all band limited by the input filters are sequentially sampled, the output of which is a PAM waveform containing samples of the input signals periodically interlaced in time. The samples from adjacent input message channels are separated by Ts/M, where M is the number of input channels. A set of M pulses consisting of one sample from each of the input M-input channels is called a frame.

At the receiver the samples from individual channels are separated by carefully synchronizing and are critical part TDM. The samples from each channel are filtered to reproduce the original message signal. There are two levels of synchronization. Frame synchronization is necessary to establish when each group of samples begin and word synchronization is necessary to properly separate the samples within each frame.

Besides the space diversity & frequency diversity there is a method of sending multiple analog signals on a channel using "TIME DIVISION MULTIPLEXING & DEMULTIPLEXING" Technique.

CIRCUIT DESCRIPTION:-

Function Generator Circuit:-

A 4.096 MHz clock is used to derive the modulating signal, which is generated by an oscillator circuit comprising a 4.096MHz crystal and three 74HC04(U2) inverter

gates. this 4.096 MHz clock is then divided down in frequency by a factor of 4096, by binary counter 74HC4040(U3), to produce 50% duty cycle, 64 KHz square wave on pin no.1 of U4, and 32KHz square wave on pin no.4. 32 KHz square wave is given to pin no.2 of IC NE555(U7) which act as a monostable multivibrator. Potentiometer P5 is used to adjust the pulse width. 64KHz square wave is fed to the four bit binary counter on pin no.1 to produce 4KHz square wave at pin no.6. this goes to pin no.13. this signal clocks to the second half of the counter to produce square wave at following frequencies.

Counter output	**Frequency**
2QD	250Hz
2QC	500Hz
2QB	1 KHz
2QA	2 KHz

Each of these square wave outputs is then fed to its own low pass filter circuits TL072 (U8, U9). Which generates corresponding sine wave outputs? The amplitude of this sine wave can be varied by potentiometers P1, P2, P3, P4 respectively. These sine wave outputs are available at TP1, TP2, TP3, and TP4 respectively and have amplitudes up to 10V max.

Transmitter Block:-

Each modulating signal is applied to IC TLO74(U6)(pin nos. 3,5,10,12 respectively). This IC buffers the applied signal and is fed to pin nos.3,14,11,6 respectively of IC DG211(U5). The pulse input(32KHz(clock)) is applied to pin nos. 1,16,9,8 of U5. Corresponding PAM outputs are available at test points Tp5,Tp6,Tp7,Tp8 respectively. These each PAM outputs are applied to IC 4052(U1). Which will act as multiplexer.

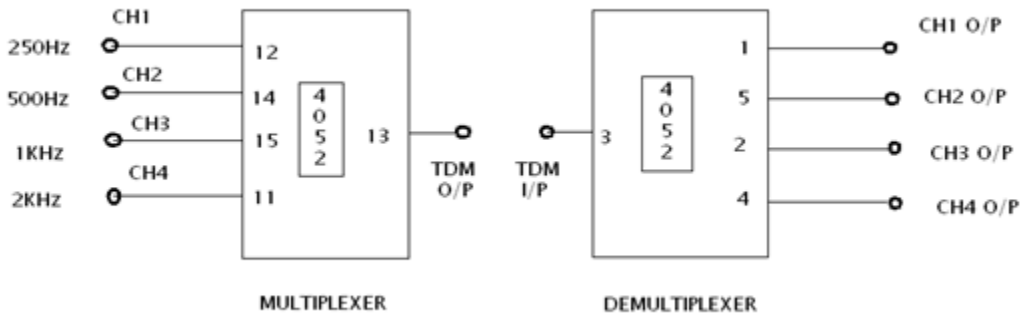
4 Channel Demultiplexer:-

The multiplexed PAM signal is given to the 4 channel Demultiplexer input at pin 3(TP12). The A& B timing wave forms selects the channel and accordingly connects the same to the output. This at the PAM signal of each channel are separated these separated demultiplexed outputs are monitored at test points 13,14,15,16 respectively.

Low Pass Filter:-

Each separated PAM outputs are being connected to corresponding channel's butter worth Low Pass Filter. This is 4^{th} order filter having roll of rate of 24db/octave(40db/decade) and cut-off frequency of 250Hz,500Hz,1KHz,2KHz respectively. The output of these filters goes to corresponding sockets termed as CH1,CH2,CH3,CH4. The reconstructed signal can be monitored at test points 17,18,19,20 respectively. These outputs are at lower amplitude.

CIRCUIT DIAGRAM:



PROGRAM:-

```
%program for time division multiplexing and demultiplexing
clc;
close all;
clear all;
% Signal generation
x=0:.5:4*pi;                    % siganal taken upto 4pi
sig1=8*sin(x);                  % generate 1st sinusoidal signal
l=length(sig1);
sig2=8*triang(l);               % Generate 2nd traingular Sigal
% Display of Both Signal
subplot(2,2,1);
plot(sig1);
title('Sinusoidal Signal');ylabel('Amplitude--->');xlabel('Time--->');
```

```
subplot(2,2,2);
plot(sig2);
title('Triangular Signal');ylabel('Amplitude--->');xlabel('Time--->');
% Display of Both Sampled Signal
subplot(2,2,3);
stem(sig1);
title('Sampled Sinusoidal Signal');
ylabel('Amplitude--->');xlabel('Time--->');
subplot(2,2,4);
stem(sig2);
title('Sampled Triangular Signal');
ylabel('Amplitude--->');xlabel('Time--->');
l1=length(sig1);
l2=length(sig2);
 for i=1:l1
  sig(1,i)=sig1(i);          % Making Both row vector to a matrix
  sig(2,i)=sig2(i);
 end
 % TDM of both quantize signal
tdmsig=reshape(sig,1,2*l1);
% Display of TDM Signal
figure
stem(tdmsig);
title('TDM Signal');ylabel('Amplitude--->');xlabel('Time--->');
 % Demultiplexing of TDM Signal
 demux=reshape(tdmsig,2,l1);
 for i=1:l1
  sig3(i)=demux(1,i);      % Converting The matrix into row vectors
  sig4(i)=demux(2,i);
 end
  % display of demultiplexed signal
```

```
figure
subplot(2,1,1)
plot(sig3);
title('Recovered Sinusoidal Signal'); ylabel('Amplitude--->');
xlabel('Time--->');
subplot(2,1,2)
plot(sig4);
title('Recovered Triangular Signal'); ylabel('Amplitude--->');
xlabel('Time--->');
```

PROCEDURE:-

Multiplexing:-

1. Connect the circuit as shown in diagram 1..
2. Switch ON the power supply.
3. Set the amplitude of each modulating signal as 5v peak-peak.
4. Monitor the outputs at test points 5,6,7,8. these are natural sampling PAM outputs.
5. Observe the outputs varying the duty cycle pot(P5). The PAM outputs will varying with 10% to 50% duty cycle.
6. Try varying the amplitude of modulating signal corresponding each channel by using amplitude pots P1, P2, P3, P4. Observe the effect on all outputs.
7. Observe the TDM output at pin no.13 (at TP9) OF 4052. All the multiplexer channel are observed during the full period of the clock(1/32 KHz).

Demultiplexing & Low Pass Filter:-

1. Connect the circuit as shown in diagram 2.
2. Observe the demultiplexed outputs at test points 13,14,15,16 respectively.
3. Observe by varying the duty cycle pot P5 and see the effect on the outputs.
4. Observe the low pass filter outputs for each channel at test points 17,18,19,20 and at sockets channels CH1, CH2, CH3, and CH4. These signals are true replica of the inputs. These signals have lower amplitude.

EXPECTED WAVEFORMS

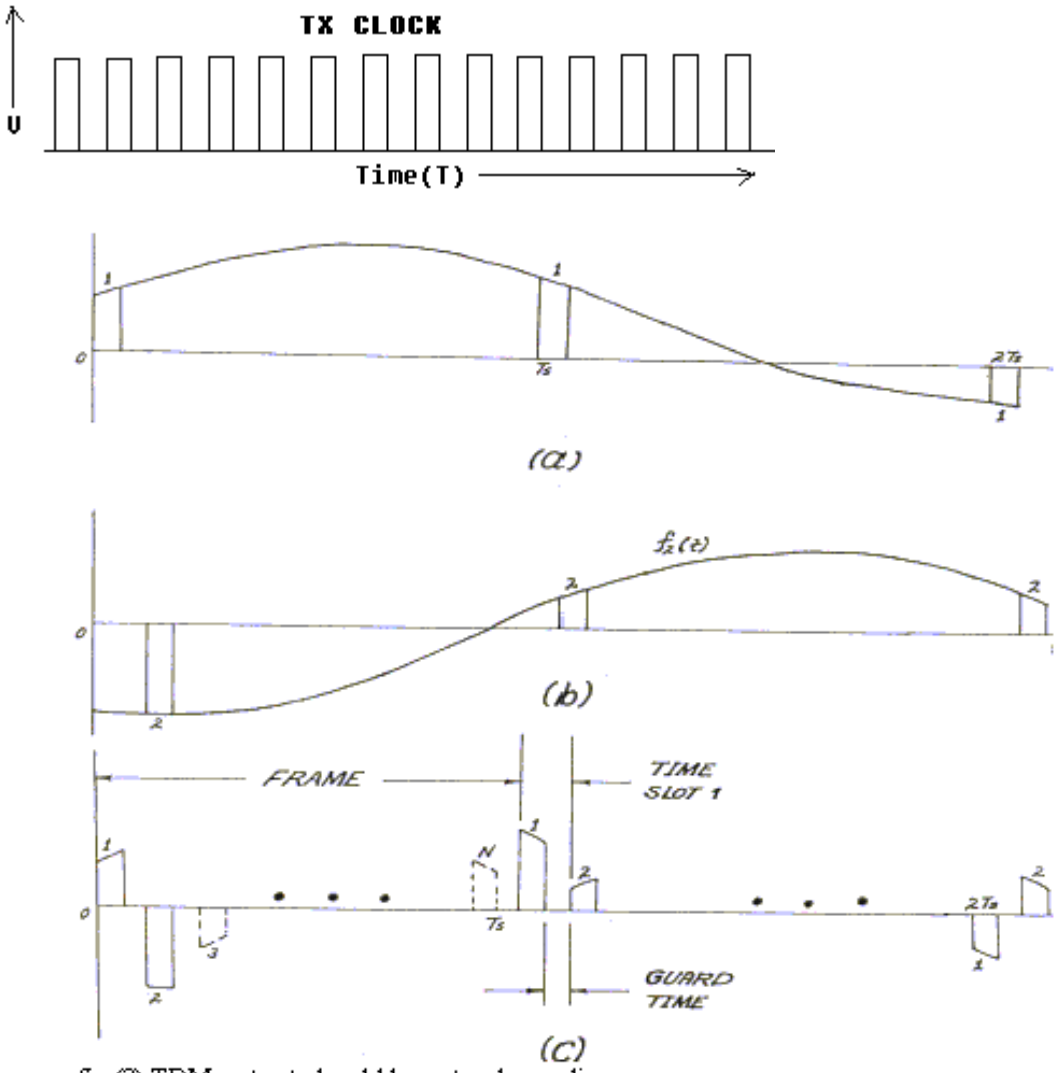


fig (2) TDM output should be natural sampling

Fig (a) message1 (b) message 2 and

RESULT:

QUESTIONS

1. Draw the TDM signal with 2 signals being multiplexed over the channel?
2. Define guard time & frame time?

3. Explain block schematic of TDM?
4. How TDM differ from FDM?
5. What type of filter is used at receiver end in TDM system?
6. What are the applications of TDM?
7. If 2 signal band limited to 3 kHz, 5 KHz & are to be time division multiplexed. What is the maximum permissible interval between 2 successive samples.?
8. Is the bandwidth requirement for TDM & FDM will be same?
9. Is TDM system is relatively immune to interference with in channels (inter channel cross talk) as compared to FDM?
10. Is the FDM susceptible to harmonic distortion compared to TDM?
11. In what aspects, TDM is superior to FDM?

EXPERIMENT NO-8 DATE:

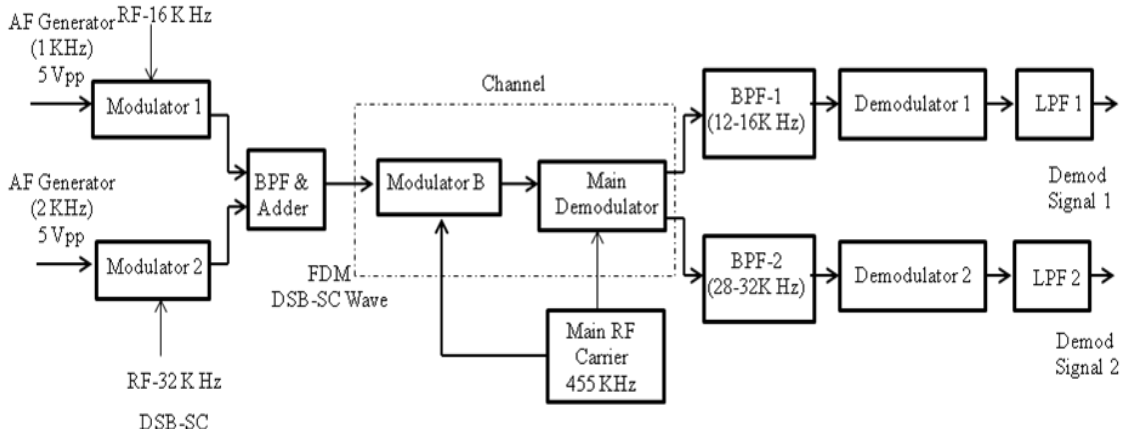
FREQUENCY DIVISION MULTIPLEXING & DE MULTIPLEXING

AIM: To study the frequency division multiplexing and De multiplexing Techniques.

APPARATUS/SOFTWARE REQUIRED:

1. FREQUENCY DIVISION MULTIPLEXING & DEMULTIPLEXING Trainer Kit.
2. C.R.O (30 MHz)
3. Patch chords.
4. PC with windows (95/98/XP/NT/2000)
5. MATLAB Software

BLOCK DIAGRAM:



PROGRAM:

```
%program for frequency division multiplexing and demultiplexing
close all
clear all
clc
Fs = 100;          % sampling freq
t = [0:2*Fs+1]'/Fs;
x1 = sin(2*pi*2*t); % signal 1 signal
z1 = fft(x1);
z1=abs(z1);
```

```
x2 = sin(2*pi*10*t); % signal 2 signal
z2 = fft(x2);
z2=abs(z2);
figure;
subplot(4,1,1); plot(x1);
title('signal 1');xlabel('time');ylabel('amplitude');
subplot(4,1,2); plot(x2);
title('signal 2');xlabel('time');ylabel('amplitude');
subplot(4,1,3); plot(z1);
title('Spectrum of signal 1');xlabel('freqency');ylabel('magnitude');
subplot(4,1,4); plot(z2);
title('Spectrum of signal 2');xlabel('freqency');ylabel('magnitude');
% freqency multiplexing
z=z1+z2;
figure;
plot(z);
title('frequency multiplexed signals');
figure;
% freqency demultiplexing
f1=[ones(10,1); zeros(182,1);ones(10,1)];%applying filter for signal 1
dz1=z.*f1;
d1 = ifft(dz1);
subplot(2,1,1)
plot(t*100,d1);
f2=[zeros(10,1); ones(182,1);zeros(10,1)];% applying filter for signal 2
dz2=z.*f2;
d2 = ifft(dz2);
title('recovered signal 1');xlabel('time');ylabel('amplitude');
subplot(2,1,2)
plot(t*100,d2);
title('recovered signal 2');xlabel('time');ylabel('amplitude');
```

PROCEDURE:

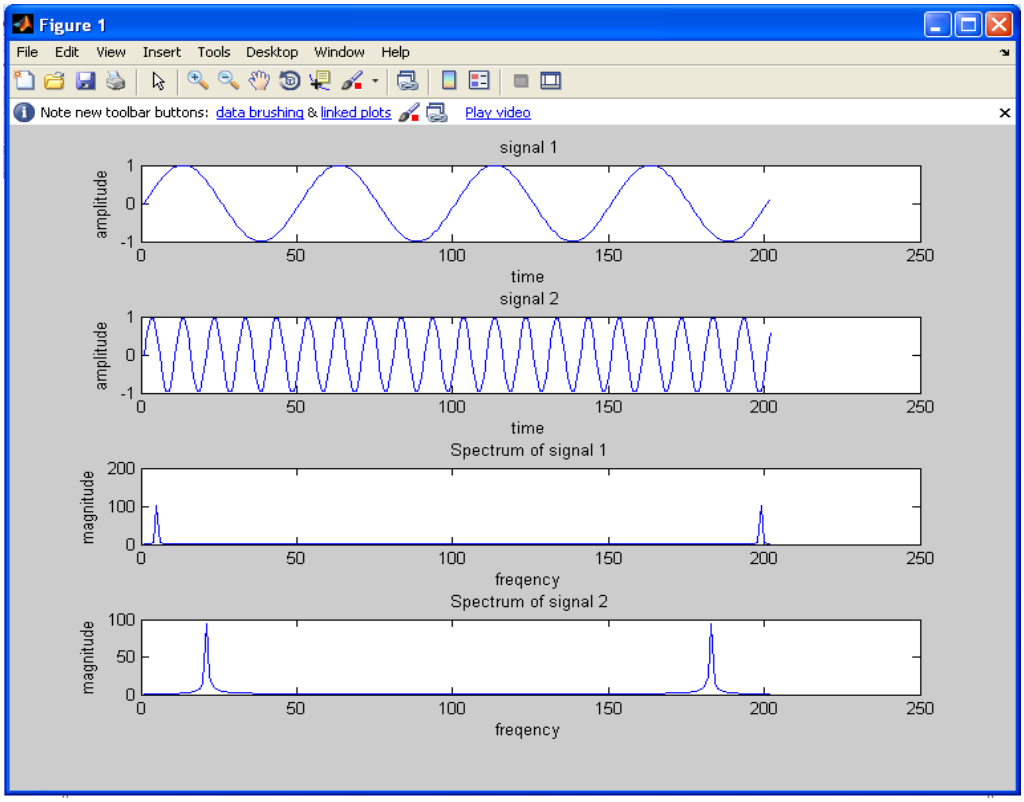
FDM Multiplexing:

1. Connect the circuit as shown in the figure.
2. Switch ON the power supply.
3. Set the amplitude of each modulating signal as 5Vp-p and frequency of each AF signal to 1kHz and 2kHz respectively.
4. Monitor the outputs at Tp1(signal-1), Tp2(signal-2),Tp10(RF-16kHz),Tp12(RF-32KHz),Tpq(modulation-1),Tp11(Modulator-2),Tp17(BPF & adder)
5. Set output frequency of RF oscillator to 455 kHz and amplitude to10Vp-p.
6. Monitor the output at Tp18 the FDM DSB-SC wave will be observed.

FDM DeMultiplexing & LPF:

1. Connect the Tp18 to Tp22 and observe the output of main demodulator at Tp23.
2. Connect the main demodulator output to the BPF1 (28-32 kHz) and BPF1 (12-16 kHz).
3. Connect the output of BPF,s to the respective demodulator and then to LPF,s.
4. Monitor the demodulated signal1 and at TP32 and demodulated signal2 atTP39.

EXPECTED WAVEFORMS:



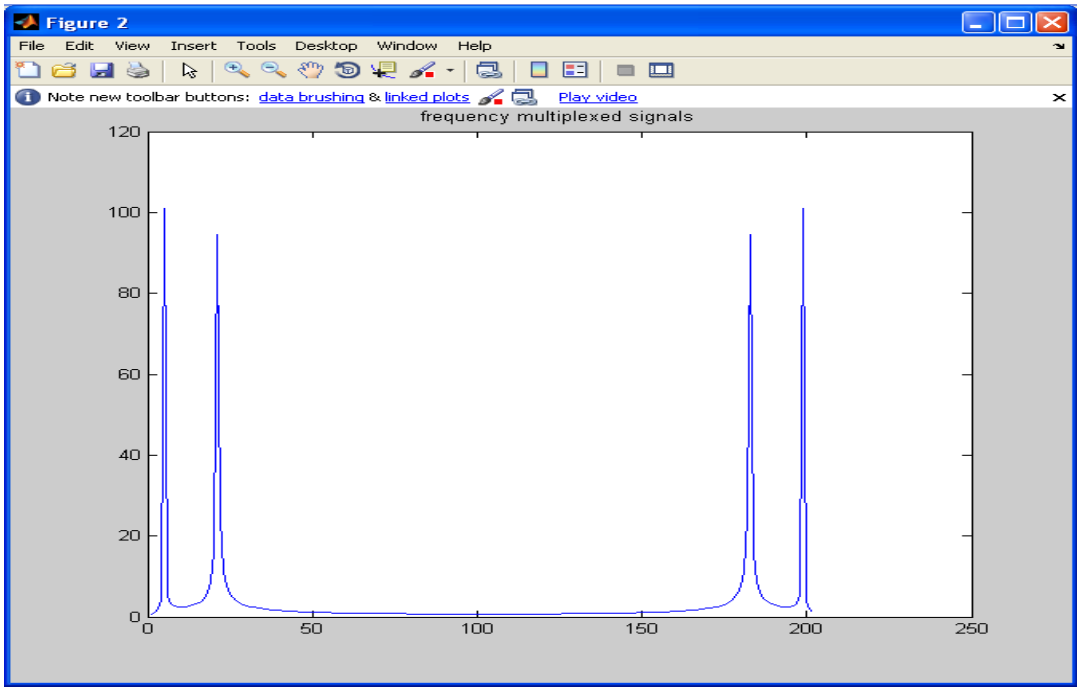


Figure 2
File Edit View Insert Tools Desktop Window Help
Note new toolbar buttons: data brushing & linked plots Play video
frequency multiplexed signals
120
100
80
60
40
20
0
0 50 100 150 200 250

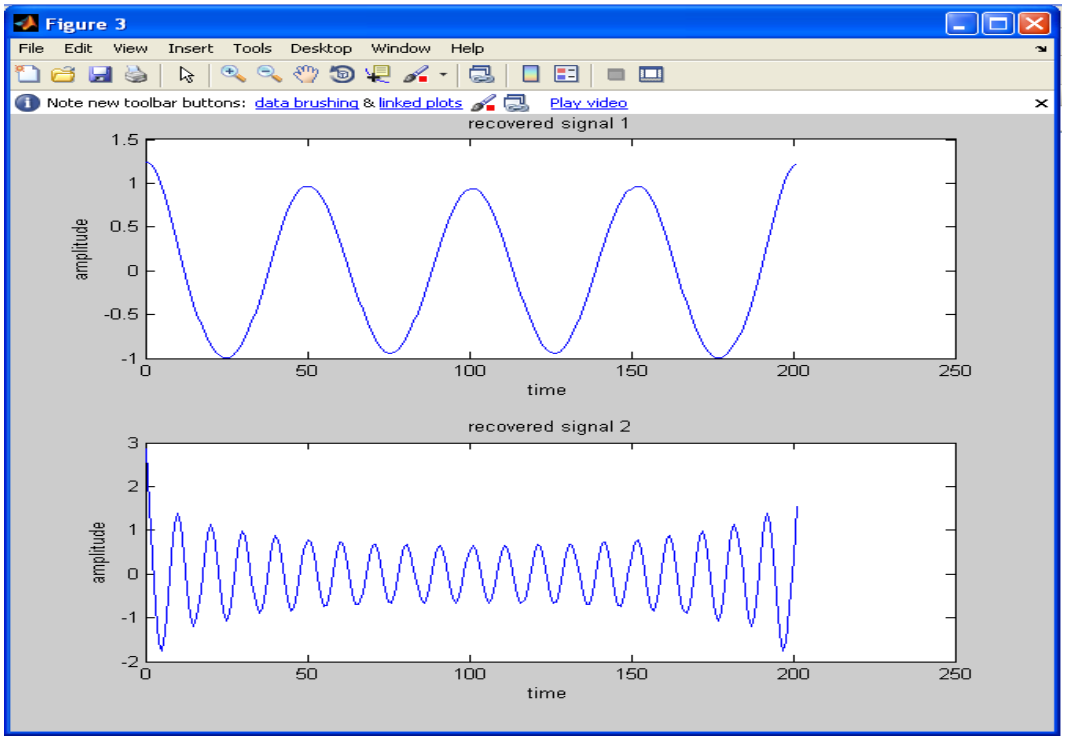


Figure 3
File Edit View Insert Tools Desktop Window Help
Note new toolbar buttons: data brushing & linked plots Play video
recovered signal 1
amplitude
1.5
1
0.5
0
-0.5
-1
0 50 100 150 200 250
time
recovered signal 2
amplitude
3
2
1
0
-1
-2
0 50 100 150 200 250
time

RESULT:

EXPERIMENT NO-9 DATE:

VERIFICATION OF SAMPLING THEOREM

AIM:

1. To study the sampling theorem and its reconstruction.

2. To study the effect of amplitude and frequency variation of modulating signal on the output.

3. To study the effect of variation of sampling frequency on the demodulated output.

APPARATUS:

1. Sampling and reconstruction Trainer Kit.
2. C.R.O(30Mhz)
3. Patch cords.
4. PC with windows(95/98/XP/NT/2000)
5. MATLAB Software with communication toolbox

THEORY:

Pulse Modulation is used to transmit analog information. In this system continuous wave forms are sampled at regular intervals. Information regarding the signal is transmitted only at the sampling times together with synchronizing signals.

At the receiving end, the original waveforms may be reconstituted from the information regarding the samples.

Sampling Theorem Statement:

A band limited signal of finite energy which has no frequency components higher than f_m Hz, is completely described by specifying the values of the signal at instants of time separated by ½ f_m seconds.

The sampling theorem states that, if the sampling rate in any pulse modulation system exceeds twice the maximum signal frequency, the original signal can be reconstructed in the receiver with minimum distortion.

$F_s > 2f_m$ is called Nyquist rate.

Where f_s – sampling frequency

F_m – Modulation signal frequency.

If we reduce the sampling frequency f_s less than f_m, the side bands and the information signal will overlap and we cannot recover the information signal simply by low pass filter. This phenomenon is called fold over distortion or aliasing.There are two methods of sampling. (1) Natural sampling (2) Flat top sampling.

Sample & Hold circuit holds the sample value until the next sample is taken. Sample & Hold technique is used to maintain reasonable pulse energy.The duty cycle of a signal is defined as the ratio of Pulse duration to the Pulse repetition period. The duty cycle of 50% is desirous taking the efficiency into account.

Circuit Description:-

Pulse and Modulating Signal Generator:-

A 4.096 MHz clock is used to derive the modulating signal, which is generated by an oscillator circuit comprising a 4.096MHz crystal and three 74HC04(U9) inverter gates. This 4.096MHz clock is then divided down in frequency by a factor of 4096, by binary counter 74HC4040(U10), to produce 50% duty cycle, 1KHz square wave on pin no.1 of U10, and 2KHz square wave on pin no.15. the frequency is selectable by means of SW1. this input of fourth order low pass filter U11(TL072) is used to produce sine wave from the square wave. The amplitude of this sine wave can be varied.

The square wave which is generated by the oscillator is buffered by inverter 74HC04(U9), to produce 32KHz square wave at pin no. 4 of the 74HC4040. This pulse is given to the monostable multi(U4) to obtain the 16KHz and 32KHz square wave at the output which are selected by the frequency pot.

Sampling Circuit:-

The IC DG211(U3) is used as analog switch which is used in pulse amplitude modulation in this circuit. The modulation signal & pulse signal are given as the input to TL074(U2), 7400(U1) IC's respectively. These IC output are fed to the inputs of the DG211.

The sampled output is available at the pin no.2 of DG211 and it is buffered by using TL074(U2) and then output is available at TP5.

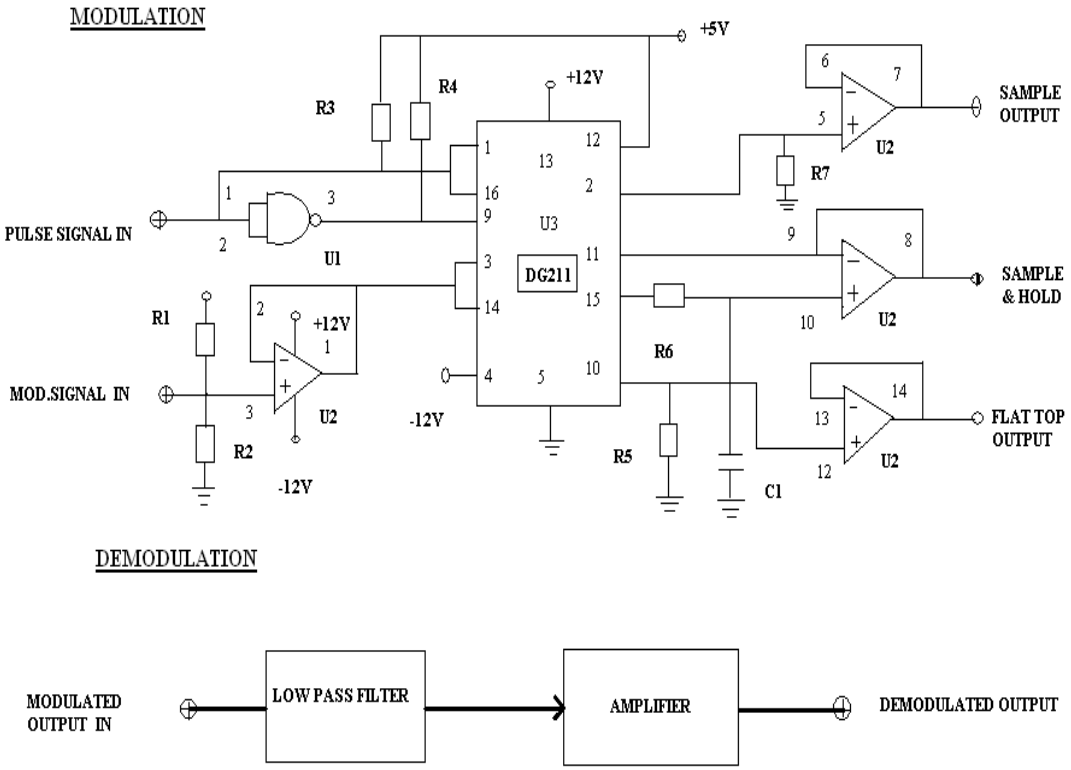
Similarly the sample & hold output and the flat top output are available at pin no15 & 10 of DG211 respectively. These are buffered by TL074(U2) and then output is available at TP6 & TP7 respectively.

Reconstruction Circuit:-

The demodulation section comprises of a fourth order low pass filter and an AC amplifier. The TL074 (U5) is used as a low pass filter and AC amplifier. The output of the modulator is given as the input to the low pass filter.

The low pass filter output is obviously less and it is fed to the AC amplifier which comprises of a single op amp and whose output is amplified.

CIRCUIT DIAGRAM:



PROGRAM:-

```
%program for verification of sampling theorem
close all;
clear all
clc
```

```
t=-10:.01:10;
 T=4;
 fm=1/T;
 x=cos(2*pi*fm*t);      % input signal
 subplot(2,2,1);
 plot(t,x);
 xlabel('time');ylabel('x(t)');title('continous time signal');
 grid;
 n1=-4:1:4;
fs1=1.6*fm;
fs2=2*fm;
fs3=8*fm;
%discrete time signal with fs<2fm
x1=cos(2*pi*fm/fs1*n1);
subplot(2,2,2);
stem(n1,x1);
xlabel('time');ylabel('x(n)');
title('discrete time signal with fs<2fm');
hold on
subplot(2,2,2);
 plot(n1,x1)
  grid;
  %discrete time signal with fs=2fm
  n2=-5:1:5;
  x2=cos(2*pi*fm/fs2*n2);
    subplot(2,2,3);
 stem(n2,x2);
 xlabel('time');ylabel('x(n)');
title('discrete time signal with fs=2fm');
 hold on
subplot(2,2,3);
```

```
plot(n2,x2)
%discrete time signal with fs>2fm
 grid;
 n3=-20:1:20;
x3=cos(2*pi*fm/fs3*n3);
subplot(2,2,4);
stem(n3,x3);
xlabel('time');ylabel('x(n)');
title('discrete time signal with fs>2fm');
 hold on
subplot(2,2,4);
 plot(n3,x3)
 grid;
```

PROCEDURE:

Sampling:-

1. Connect the circuit as shown in diagram 1 .

   a. The output of the modulating signal generator TP1 is connected to modulating signal input TP4 of the sampling circuit keeping the frequency switch in 1KHz position, and amplitude knob to max position.

   b. The output of pulse generator TP2 is connected to sampling pulse input TP3 of the sampling circuit keeping the frequency switch in 16KHz position.(Adjust the duty cycle pot to mid position i.e.50%).

2. Switch ON the power supply.
3. Observe the outputs of sampling, sampling and hold, flat top output at TP7, TP8 and TP9 respectively. By varying the amplitude pot also observe the effect on outputs.
4. By varying Duty cycle pot observe the effect on sampling outputs (Duty cycle is varying from 10-15%).

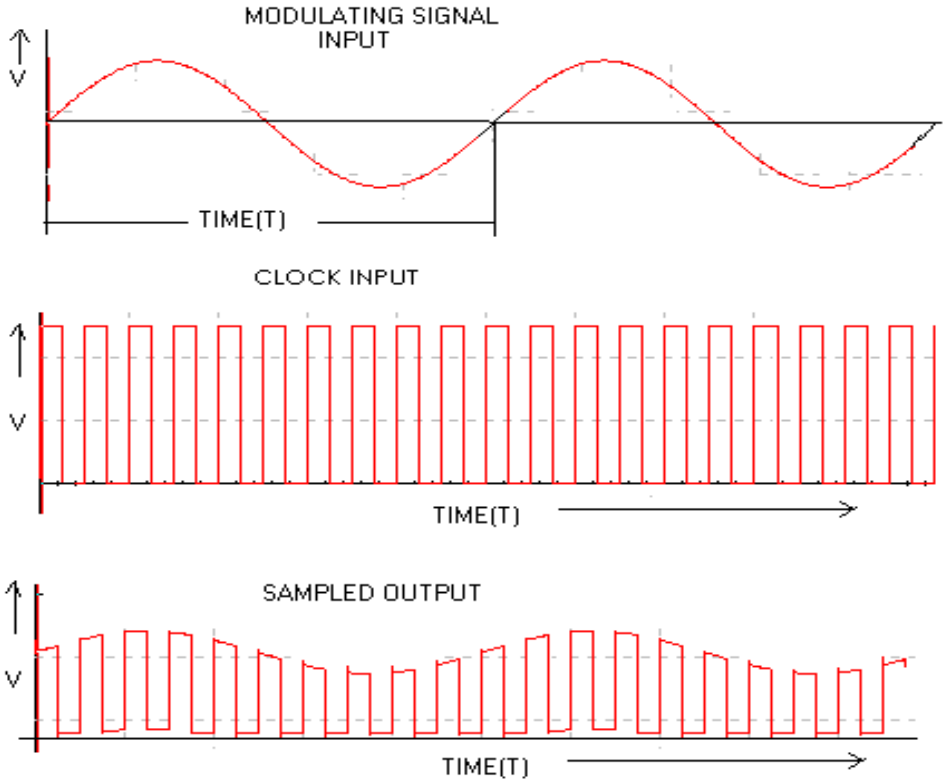
5. Vary the switch position in the pulse generator circuit to 32 KHz and now observe the outputs at TP7, TP8 and TP9.By varying the amplitude pot also observe the effect on outputs.
6. Now, vary the switch position in modulating signal generator to 2 KHz and repeat all the above steps 3&4.
7. Switch OFF the power supply.

Reconstruction:-

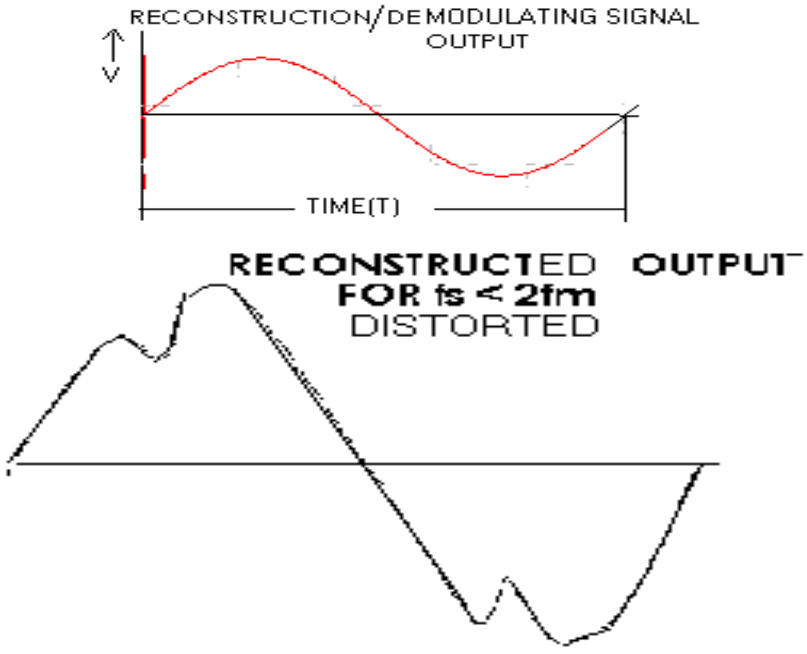
1. Connect the circuit as shown in diagram 2.
    a. . The output of the modulating signal generator TP1 is connected to modulating signal input TP4 of the sampling circuit keeping the frequency switch in 1 KHz position, and amplitude knob to max position.
    b. The output of pulse generator TP2 is connected to sampling pulse input TP3 of the sampling circuit keeping the frequency switch in 16KHz position.(Adjust the duty cycle pot to mid position i.e.50%).
    c. Connect the sample output from TP7 to the input of low pass filter TP10.
    d. Output of low pass filter from TP11 to input of AC amplifier TP12, keep the gain pot in AC amplifier to max position.
2. Switch ON the power supply.
3. Observe the output of AC amplifier at TP13. The output will be the replica of the input. By varying the gain pot observe the demodulating signal amplification.
4. Similarly connect the sample and hold output and flat top output to TP10 and observe reconstructed the signal.
5. Vary the switch position in the sampling frequency circuit to 32KHz and now repeat the steps 3&4.
6. Vary the switch position in the modulating signal generator to 2KHz and repeat all the above steps 3 to 5.
7. Switch OFF the power supply.

EXPECTED WAVEFORMS:

Below Wavforms for **fs > 2fm**



Demodulated Output



RESULT:

QUESTIONS

1. What are the types of sampling?
2. State sampling theorem?
3. What happens when fs < 2 fm?
4. How will be the reconstructed signal when fs >= 2fm?
5. Explain the operation of sampling circuit?
6. Explain the operation of re-construction circuit?
7. Who formalized the sampling theorem?
8. What are the applications of the above theorem?
9. Is the sampling theorem basis for the modern digital communications?
10. Is the voice signal sampling of 8000 Hz, follows sampling theorem in Land line Telephone Exchange.

EXPERIMENT NO-10 DATE:

PULSE AMPLITUDE MODULATION

AIM:- 1.To study the Pulse amplitude modulation & demodulation Techniques.

2. To study the effect of amplitude and frequency variation of modulating signal on the output.

APPARATUS:-

1. Pulse amplitude modulation & demodulation Trainer Kit.
2. Dual trace CRO.
3. Patch chords.
4. PC with windows(95/98/XP/NT/2000)
5. MATLAB Software with communication toolbox

THEORY:-

Pulse modulation is used to transmit analog information. In this system continuous wave forms are sampled at regular intervals. Information regarding the signal is transmitted only at the sampling times together with syncing signals.

At the receiving end, the original waveforms may be reconstituted from the information regarding the samples.

The pulse amplitude modulation is the simplest form of the pulse modulation. PAM is a pulse modulation system is which the signal is sampled at regular intervals, and each sample is made proportional to the amplitude of the signal at the instant of sampling. The pulses are then sent by either wire or cables are used to modulated carrier.

The two types of PAM are i) Double polarity PAM, and ii) the single polarity PAM, in which a fixed dc level is added to the signal to ensure that the pulses are always positive. Instantaneous PAM sampling occurs if the pulses used in the modulator are infinitely short.

Natural PAM sampling occurs when finite-width pulses are used in the modulator, but the tops of the pulses are forced to follow the modulating waveform.

Flat-topped sampling is a system quite often used because of the ease of generating the modulated wave.

PAM signals are very rarely used for transmission purposes directly. The reason for this lies in the fact that the modulating information is contained in the amplitude factor of the pulses, which can be easily distorted during transmission by noise, crosstalk, other forms of distortion. They are used frequently as an intermediate step in other pulse-modulating methods, especially where time-division multiplexing is used.

Circuit description:-

Pulse and Modulation Signal Generator:-

A 4.096 MHz clock is used to derive the modulating signal, which is generated by an oscillator circuit comprising a 4.096MHz crystal and three 74HC04(U9) inverter gates. This 4.096MHz clock is then divided down in frequency by a factor of 4096, by binary counter 74HC4040(U10), to produce 50% duty cycle, 1 KHz square wave on pin no.1 of U10, and 2KHz square wave on pin no.15. the frequency is selectable by means of SW1. this goes to input of fourth order low pass filter U11(TL072) is used to produce sine wave from the square wave. The amplitude of this sine wave can be varied.

The square wave which is generated by the oscillator is buffered by inverter 74HC04(U9), to produce 32KHz square wave at pin no.4 of the 74HC4040(U10). This pulse is given to the monostable multi to obtain the 16 KHz and 32 KHz square wave at the output which are selected by the frequency pot.

Modulation:-

The ICDG211 (U3) is used as a pulse amplitude modulation in this circuit. The modulation signal & pulse signals are given to TL074 (U2) & 7400(U1) IC's respectively. These outputs are fed to the inputs the D4211 (U3).

The sampled output is available at the pin no 2 of DG211 and it is buffered by using TL074 (U2) and then output is available at TP5.

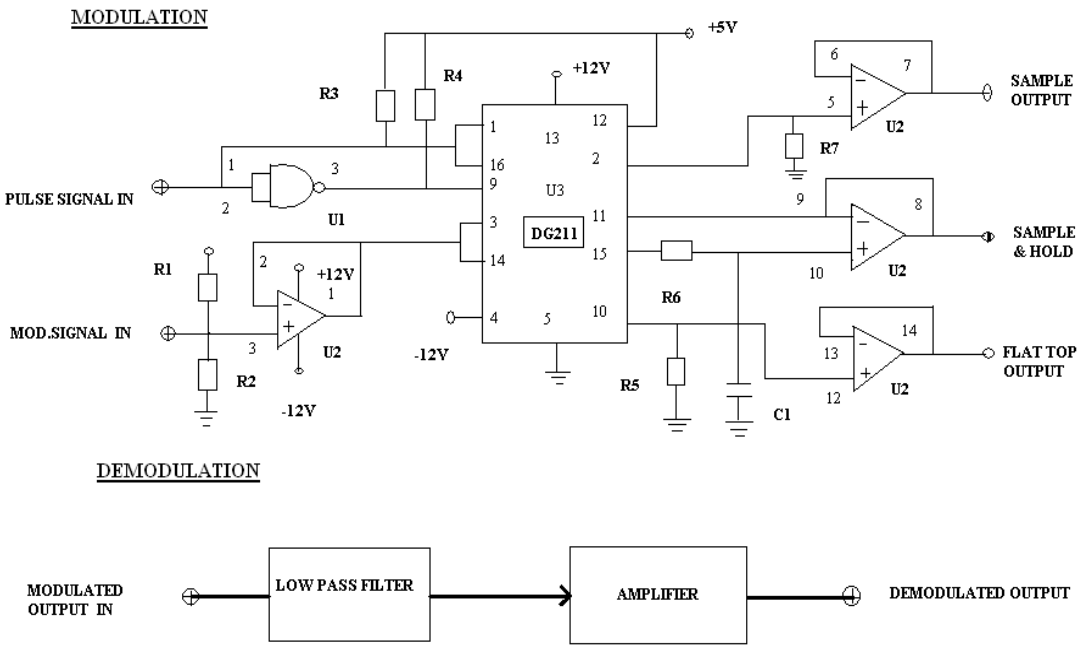
Similarly the sample & hold output and the flat top output are available at pin no.15 &10 of DG211 respectively. These are buffered by TL074 (U2) and then output is available at TP6&TP7 respectively.

Demodulation:-

The demodulation section comprises of fourth order low pass filter and an AC amplifier. The TL074 (U5) is used as a low pass filter and AC amplifier. The output of the modulator is given as the input to the low pass filter.

The low pass filter output is obviously less and it is fed to the AC amplifier which comprises of a single op amp and whose output is amplified.

CIRCUIT DIAGRAM:



PROGRAM:-

```
% pulse amplitude modulation
close all
clear all
clc
t = 0 : 1/1e3 : 10;        % 1 kHz sample freq for 1 sec
d = 0 : 1/5 : 10;
x = 5+sin(2*pi/4*2*t);      %message signal
figure;
subplot(3,1,1)
plot(x);
```

```
title('message');
xlabel('time');ylabel('amplitude');
y = pulstran(t,d,'rectpuls',0.1); %generation of pulse input
subplot(3,1,2)
plot(y);
title('Pulse Input ');
xlabel('time');ylabel('amplitude');
z=x.*y;                % PAM output
subplot(3,1,3)
plot(z);
title('PAM modulation ');
xlabel('time');ylabel('amplitude');
```

PROCEDURE:

Double Polarity:-

Modulation:-

1. Connect the circuit as shown in diagram 1.
    a. The output of the modulating signal generator is connected to the modulating signal input TP2 keeping the frequency switch in 1KHz position, and amplitude knob to max position
    b. 16KHz pulse output to pulse input TP1.(Keep the frequency in minimum position in pulse generator block).
2. Switch ON the power supply.
3. Monitor the outputs at TP5, TP6& TP7. And observe the outputs also by varying amplitude pot (Which is in modulation signal generator block).
4. Now vary the frequency selection which position in modulating signal generator block to 2 KHz, amplitude pot to max position.
5. Observe the output at TP5, TP6& TP7 and observe the outputs also by varying amplitude pot (Which is in modulation signal generator block).
6. Repeat all the above steps for the pulse frequency 32KHz (By varying the frequency pot in the pulse generator block).
7. Switch OFF the power supply.

Single Polarity PAM:-

8. Connect the circuit as shown in diagram 2.

a. The output of the modulating signal generator is connected to the modulating signal input TP2 keeping the frequency switch in 1KHz position, and amplitude knob to max position

b. 16KHz pulse output to pulse input TP1 .

9. Switch ON the power supply.

10. Repeat above step 3 to 6 and observe the outputs.

11. Vary DC output pot until you get single polarity PAM at TP5, TP6, TP7.

12. Switch OFF the power supply.

Demodulation:-

1. Connect the circuit as shown in diagram 3.

a. The output of the modulating signal generator is connected to the modulating signal input TP2 keeping the frequency switch in 1KHz position, and amplitude knob to max position

b. 16KHz pulse output to pulse input TP1.

c. Sample output, sample and hold output and flat top outputs Respectively to the input of low pass filter(TP9) and LPF output (TP10) to AC amplifier input(TP11).

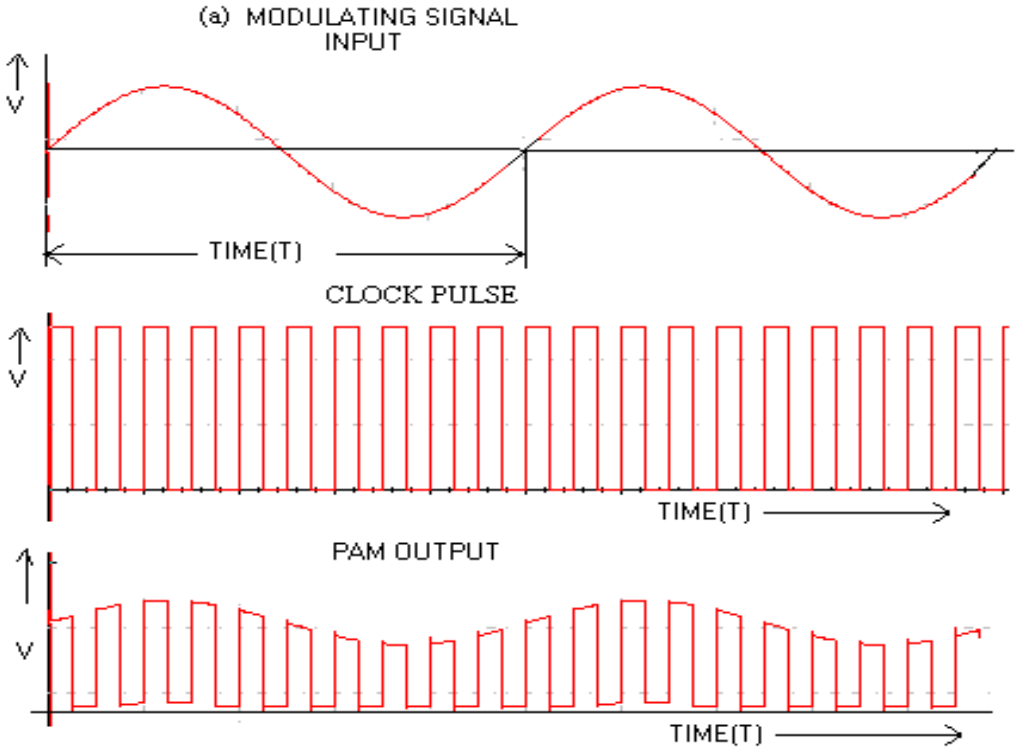
2. Observe the output of LPF and AC amplifier at TP10,TP12 respectively, corresponding to inputs from TP5,TP6 &TP7. The outputs will be the true replica of the input.

3. Now, set the switch position in modulating signal generator to 2KHz and observe the outputs at TP10&TP12 respectively, corresponding to inputs from TP5,TP6& TP7.

4. Vary the frequency of pulse to 32KHz (By varying the frequency pot(Put in max position) in pulse generator block) and repeat the above steps 2&3.

5. Switch OFF the power supply.

EXPECTED WAVEFORMS



RESULT:

QUESTIONS

1. TDM is possible for sampled signals. What kind of multiplexing can be used in continuous modulation systems?

2. What is the minimum rate at which a speech signal can be sampled for the purpose of PAM?

3. What is cross talk in the context of time division multiplexing?

4. Which is better, natural sampling or flat topped sampling and why?

5. Why a dc offset has been added to the modulating signal in this board? Was it essential for the working of the modulator? Explain?

6. If the emitter follower in the modulator section saturates for some level of input signal, then what effect it will have on the output?

7. Derive the mathematical expression for frequency spectrum of PAM signal.

8. Explain the modulation circuit operation?
9. Explain the demodulation circuit operation?
10. Is PAM & Demodulation is sensitive to Noise?

EXPERIMENT NO-11 DATE:

PULSE WIDTH MODULATION & DEMODULATION

AIM:

1. To study the Pulse Width Modulation (PWM) and Demodulation Techniques.

2. To study the effect of Amplitude and Frequency of Modulating Signal on PWM output.

APPARATUS:

1. PWM trainer kit
2. C.R.O(30MHz)
3. Patch Chords.
4. PC with windows(95/98/XP/NT/2000)
5. MATLAB Software with communication toolbox

THEORY:-

Pulse modulation is used to transmit analog information. In this system continuous wave forms are sampled at regular intervals. Information regarding the signal is transmitted only at the sampling times together with synchronizing signals.

At the receiving end, the original waveforms may be reconstituted from the information regarding the samples.

The pulse Width Modulation of the PTM is also called as the Pulse Duration Modulation (PDM) & less often Pulse length Modulation (PLM).

In pulse Width Modulation method, we have fixed and starting time of each pulse, but the width of each pulse is made proportional to the amplitude of the signal at that instant.

This method converts amplitude varying message signal into a square wave with constant amplitude and frequency, but which changes duty cycle to correspond to the strength of the message signal.

Pulse-Width modulation has the disadvantage, that its pulses are of varying width and therefore of varying power content. This means that the transmitter must be powerful

enough to handle the maximum-width pulses. But PWM still works if synchronization between transmitter and receiver fails, whereas pulse-position modulation does not.

Pulse-Width modulation may be generated by applying trigger pulses to control the starting time of pulses from a mono stable multivibrator, and feeding in the signal to be sampled to control the duration of these pulses.

When the PWM signals arrive at its destination, the recovery circuit used to decode the original signal is a sample integrator (LPF).

CIRCUIT DESCRIPTION:-

Pulse & Modulating Signal Generator:-

A 4.096MHz clock is used to derive the modulating signal, which is generated by an oscillator circuit comprising a 4.096MHz crystal and three 74HC04(U9) inverter gates. This 4.096MHz clock is then divided down in frequency by a factor of 4096, by binary counter 74HC4040(U2), to produce 50% duty cycle, 1KHz square wave on pin no.1 of U4, and 2KHz square wave on pin no.15. the frequency is selectable by means of SW1. This goes to input of fourth order low pass filter U3 is used to produce sine wave from the square wave. The amplitude of this sine wave can be varied.

The square wave which is generated by the oscillator is buffered by inverter 74HC04, to produce 32KHz square wave at pin no.4 of the 74HC4040(U2). This pulse is given to the monostable multi to obtain the 16KHz and 32KHz square wave at the output which are selected by the frequency pot.

Modulation:-

The PWM circuit uses the 555 IC (U1) in monostable mode. The Modulating signal input is applied to pin no.5 of 555IC, and there Pulse input is applied to pin no.2.

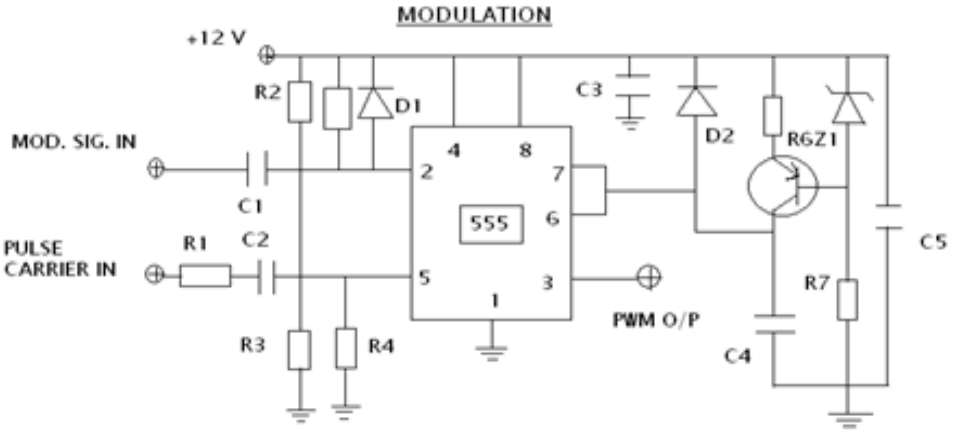
The output of PWM is taken at the pin no.3 of 555IC i.e., TP3.

Demodulation:-

The demodulation section comprises of a fourth order low pass filter and an AC amplifier. The TL074(U5) is used as a low pass filter and an AC amplifier. The output of the modulator is given as the input to the low pass filter.

The low pass filter output is obviously less and it is feed to the AC amplifier which comprises of a single op amp and whose output is amplified.

CIRCUIT DIAGRAM:



PROGRAM:-

```
% pulse width modulation & demodulation
close all
clear all
clc
fc=1000;
fs=10000;
f1=200;
t=0:1/fs:((2/f1)-(1/fs));
x1=0.4*cos(2*pi*f1*t)+0.5;
%modulation
y1=modulate(x1,fc,fs,'pwm');
subplot(311);
plot(x1);
axis([0 50 0 1]);
title('original signal taken mesage,f1=500,fs=10000')
subplot(312);
plot(y1);
axis([0 500 -0.2 1.2]);
```

```
title('PWM')
 %demodulation
x1_recov=demod(y1,fc,fs,'pwm');
subplot(313);
plot(x1_recov);
title('time domain recovered, single tone,f1=200')
axis([0 50 0 1]);
```

PROCEDURE:

Modulation:-

1. Connect the circuit as shown in the diagram 1.
    a. The output of the modulating signal generator is connected to the modulating signal input TP2 keeping the frequency switch in 1KHz position, and amplitude knob to max position
    b. 16KHz pulse output (by varying the frequency pot (put it min position) in pulse generator block) from pulse generator to pulse input(TP1).
2. Switch ON the power supply.
3. Observe the output of pulse width modulation block at TP3.(By varying the amplitude pot).
4. Vary the modulating signal generator frequency by switching the frequency selector switch to 2 KHz.
5. Now, again observe the PWM output at TP3.(By varying the amplitude pot).
6. Repeat the above steps (3 to 5) for the pulse frequency of 32KHz(by varying the frequency pot(put it in max position) in pulse generator block).
7. Switch OFF the power supply.

Demodulation:-

8. Connect the circuit as shown in diagram 2.

a. The output of the modulating signal generator is connected to the modulating signal input TP2 keeping the frequency switch in 1KHz position, and amplitude knob to max position.

b. 16KHz pulse output (put frequency pot minimum) from pulse generator block to pulse input TP1.

c. PWM output to LPF input.

d. LPF output to AC amplifier input.

9. Switch ON the power supply.

10. Observe the output of low pass filter and AC amplifier respectively at TP6 & TP8. The output will be the true replica of the input.

11. Now vary the position of the switch in modulating signal generator to 2 KHz and observe the outputs at TP6 & TP8.

12. Repeat the steps 10& 11 for pulse frequency 32 KHz (By varying the frequency pot (put in max). in pulse generator block). Observe the output waveforms.

13. Switch OFF the power supply.

EXPECTED WAVEFORMS

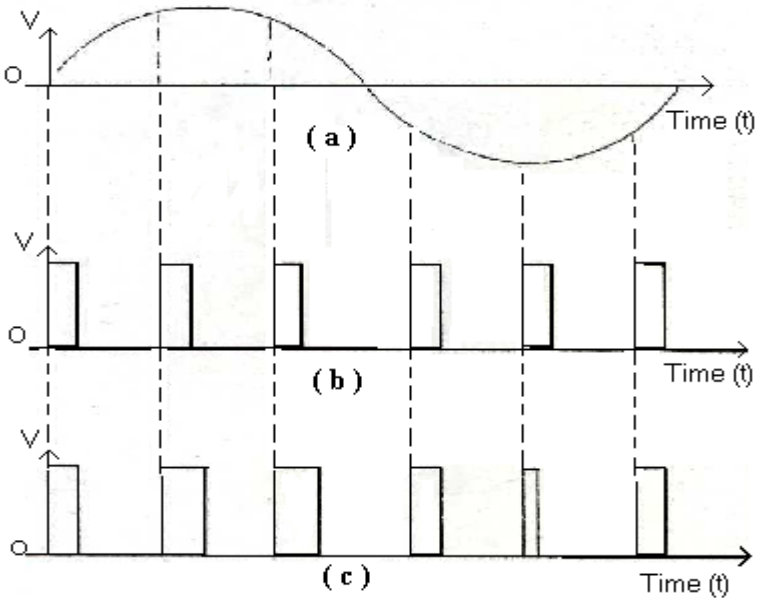


Fig (2) PULSE WIDTH MODULATION
(a) Signal
(b) Unmodulated pulses
(c) PWM

RESULT:

QUESTIONS

1. An audio signal consists of frequencies in the range of 100Hz to 5.5KHz.What is the minimum frequency at which it should be sampled in order to transmit it through pulse modulation?

2. Draw a TDM signal which is handling three different signals using PWM?

3. What do you infer from the frequency spectrum of a PWM signal?

4. Clock frequency in a PWM system is 2.5 kHz and modulating signal frequency is 500Hzhowmany pulses per cycle of signal occur in PWM output? Draw the PWM signal?

5. Why should the curve for pulse width Vs modulating voltage be linear?

6. What is the other name for PWM?

7. What is the disadvantage of PWM?

8. Will PWM work if the synchronization between Tx and Rx fails?

9. Why integrator is required in demodulation of PWM?

10. What kind of conversion is done in PWM generation?

EXPERIMENT NO-12 DATE:

PULSE POSITION MODULATION AND DEMODULATION

AIM:

1. To study the generation Pulse Position Modulation (PPM) and Demodulation.
2. To study the effect of Amplitude and the frequency of modulating signal on its output and observe the wave forms.

APPARATUS:

1. Pulse Position Modulation (PPM) and demodulation Trainer Kit.
2. C.R.O(30MHz)
3. Patch chords.
4. PC with windows(95/98/XP/NT/2000)
5. MATLAB Software with communication toolbox

THEORY:-

Pulse Modulation is used to transmit analog information in this system continuous wave forms are sampled at regular intervals. Information regarding the signal is transmitted only at the sampling times together with synchronizing signals.

At the receiving end, the original waveforms may be reconstituted from the information regarding the samples. Pulse modulation may be subdivided in to two types analog and digital. In analog the indication of sample amplitude is the nearest variable. In digital the information is a code.

The pulse position modulation is one of the methods of the pulse time modulation.PPM is generated by changing the position of a fixed time slot.

The amplitude& width of the pulses is kept constant, while the position of each pulse, in relation to the position of the recurrent reference pulse is valid by each instances sampled value of the modulating wave. Pulse position modulation into the category of analog communication. Pulse-Position modulation has the advantage of requiring constant transmitter power output, but the disadvantage of depending on transmitter receiver synchronization.

Pulse-position modulation may be obtained very simply from PWM. However, in

PWM the locations of the leading edges are fixed, whereas those of the trailing edges are not. Their position depends on pulse width, which is determined by the signal amplitude at that instant. Thus, it may be said that the trailing edges of PWM pulses are, in fact, position-modulated. This has positive-going narrow pulses corresponding to leading edges and negative-going pulses corresponding to trailing edges. If the position corresponding to the trailing edge of an un modulated pulse is counted as zero displacement, then the other trailing edges will arrive earlier or later. They will therefore have a time displacement other than zero; this time displacement is proportional to the instantaneous value of the signal voltage. The differentiated pulses corresponding to the leading edges are removed with a diode clipper or rectifier, and the remaining pulses, is position-modulated.

Circuit Description:-

Modulating Signal Generator:-

A 4.096 MHz clock is used to derive the modulating signal, which is generated by an oscillator circuit comparing a 4.096MHz crystal and three 74HC04(U9) inverter gates. This 4.096 MHz clock is then divided down in frequency by a factor of 4096, by binary counter 74HC4040(U4), to produce 50% duty cycle, 1 KHz square wave on pin no.1 of U4, and 2 KHz square wave on pin no.15. The frequency is selectable by means of SW1. This goes to input of fourth order low pass filter U3 (TL072) is used to produce sine wave from the square wave. The amplitude of this sine wave can be varied.

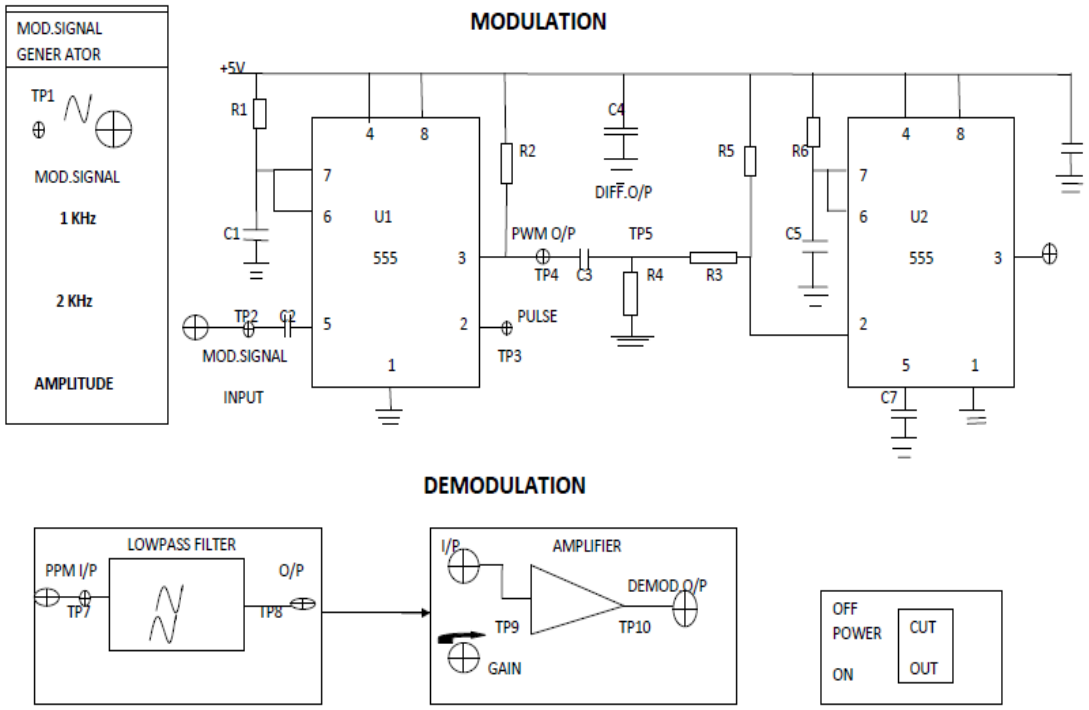
Modulation:-

The circuit uses the IC 555(U1) a Mono stable Multivibrator to perform the pulse position Modulation action.

The Modulating signal is given to Pin No. 5 at Pin No.2 the pulse is 32 KHz which is connected internally.

The PWM is available at TP2; this PWM output is differentiated by using differentiated circuit. This differentiated output is available at TP8. This differentiated output is fed to the 555 IC (U2) (Mono stable Mode) Pin No.2. The PPM output is available at TP3.

CIRCUIT DIAGRAM:



PROGRAM:-

```
% pulse position modulation
close all
clear all
clc
fc=100;
fs=1000;
f1=80;
t=0:1/fs:((2/f1)-(1/fs));
x1=0.4*cos(2*pi*f1*t)+0.5;
%modulation
y1=modulate(x1,fc,fs,'ppm');
subplot(311);
plot(x1);
axis([0 15 0 1]);
```

```
title('original signal taken mesage,f1=80,fs=1000')
subplot(312);
plot(y1);
axis([0 250  -0.2 1.2]);
title('PPM')
 %demodulation
x1_recov=demod(y1,fc,fs,'ppm');
subplot(313);
plot(x1_recov);
title('time domain recovered, single tone,f1=80')
axis([0 15 0 1]);
```

PROCEDURE:

Modulation:

1. Connect the circuit as shown in diagram 1.
    a. Connect the modulating signal generator output to modulating signal input (TP1) in PPM block.
    b. Keep the switch in 1 KHz position and amplitude pot in max position.
2. Switch ON the power supply
3. Observe the PWM output at TP2, and the differentiated output signal at TP8.
4. Now, monitor the PPM output at TP3.
5. Try varying the amplitude and frequency of sine wave by varying amplitude pot.
6. Repeat Step 5 for frequency of 2 KHz and observe the PPM output.
7. Switch OFF the power supply.

Demodulation:-

8. Connect the circuit as shown in diagram2.
    a. Connect the modulating signal generator output to modulating signal input (TP1) in PPM block.
    b. Keep the switch in 1 KHz position and amplitude pot in max position.
    c. Connect the PPM output (TP3) to input of LPF(TP4).
9. Switch ON the power supply
10. Observe the demodulated signal at the output of LPF at TP5.

11. Thus the recovered signal is true replica of the input signal

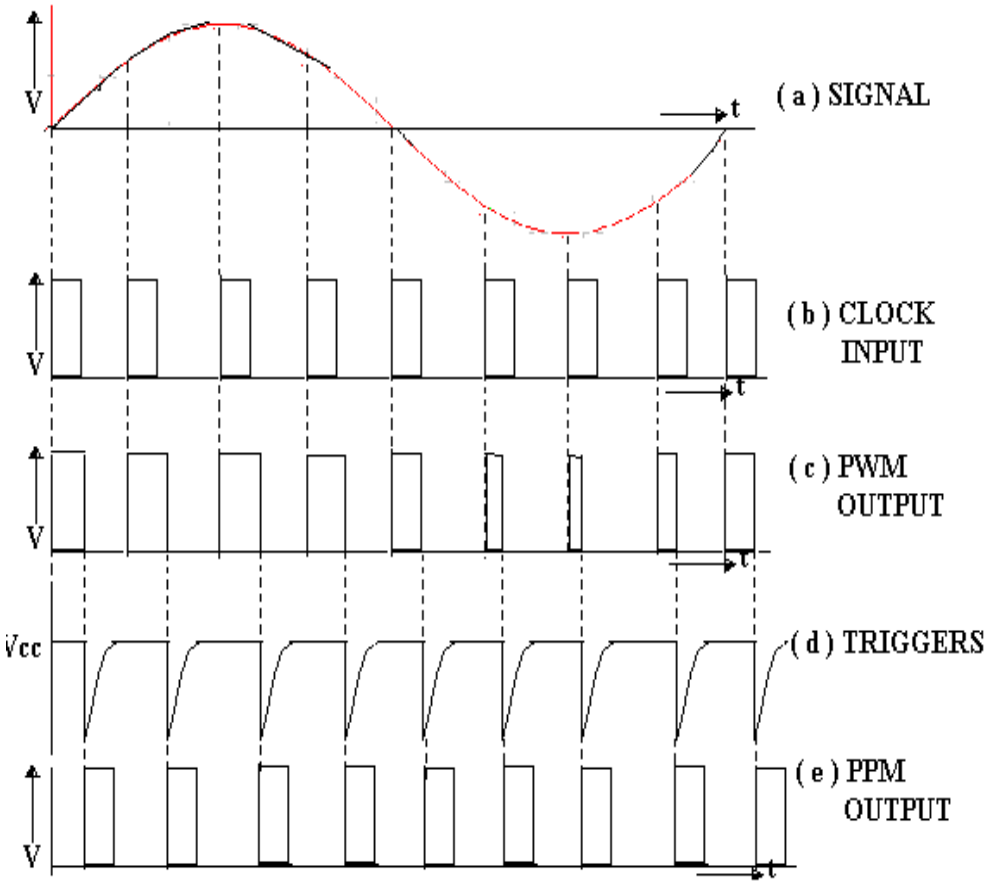
12. a. As the output of LPF has less amplitude, connect the output of LPF to the input of an AC amplifier (TP5 to TP6).

b. Observe the demodulated out put on the oscilloscope at TP7 and also observe the amplitude of demodulated signal by varying gain pot. This is amplitude demodulated output.

13. Repeat the steps (7 to 9) for the modulating signal for frequency 2 KHz.

14. Switch OFF the power supply.

EXPECTED WAVEFORMS:



RESULT:

QUESTIONS:

1. What is the advantage of PPM over PWM?
2. Is the synchronization is must between Tx and Rx
3. Shift in the position of each pulse of PPM depends on what?

4. Can we generate PWM from PPM?

5. Why do we need 555 timers?

6. Does PPM contain derivative of modulating signal compared to PWM?

7. For above scheme, do we have to use LPF and integrator in that order?

8. If we convert PPM to PWM & then detect the message signal, will the o/p has less distortion?

9. Is synchronization critical in PPM?

10. How robust is the PPM to noise?

EXPERIMENT.NO-13 DATE:

FREQUENCY SYNTHESIZER

AIM: To study the operation of frequency synthesizer using PLL

APPARATUS :

1. Frequency synthesizer trainer Kit.
2. Dual trace C.R.O (20 MHZ)
3. Digital frequency counter or multimeter
4. Patch chords
5. PC with windows(95/98/XP/NT/2000)
6. MATLAB Software with communication toolbox

THEORY:

PLL stands for 'Phase locked loop' and it is basically a closed loop frequency control system, whose functioning is based on phase sensitive detection of phase difference between the input and output signals of controller oscillator.

Before the input is applied the PLL is in free running state. Once the input frequency is applied the VCO frequency starts change and phase locked loop is said to be in captured mode. The VCO frequency continues to change until it equals the input frequency and PLL is then in the phase locked state. When phase locked the loop tracks any change in the input frequency through its repetitive action.

Frequency Synthesizer:

The frequency divider is inserted between the VCO and the phase comparator. Since the output of the divider is locked to the input frequency f_{in}, VCO is running at multiple of the input frequency. The desired amount of multiplication can be obtained by selecting a proper divide by N network. Where N is an integer. For example $f_{out} = 5\ f_{in}$ a divide by N=10, 2 network is needed as shown in block diagram. This function performed by a 4 bit binary counter 7490 configured as a divide by 10, 2 circuit. In this circuit transistor Q1 used as a driver stage to increase the driving capacity of LM565 as shown in fig.b.

To verify the operation of the circuit, we must determine the input frequency range and then adjust the free running frequency F_{out} of VCO by means of R_1 (between

10^{th} and 8^{th} pin) and CI (9^{th} pin), so that the output frequency of the 7490 driver is midway within the predetermined input frequency range. The output of the VCO now should $5F_{in.}$

Free running frequency(f_0):

Where there is no input signal applied, it is in free running mode.

$F_0 = 0.3 / (R_tC_t)$ where R_t is the timing resistor

C_t is the timing capacitor.

Lock range of PLL(f_L)

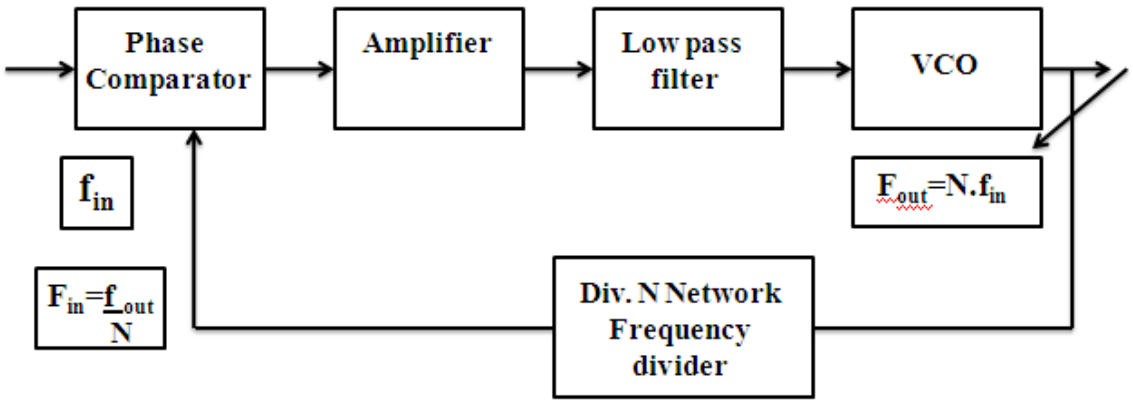
$F_L = \pm 8f_0/V_{cc}$ where f_0 is the free running frequency

$=2V_{CC}$

Capture range (f_C)

$$f_c = \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{3.6X10^3XC_c}}$$

CIRCUIT DIAGRAM:



PROGRAM:-

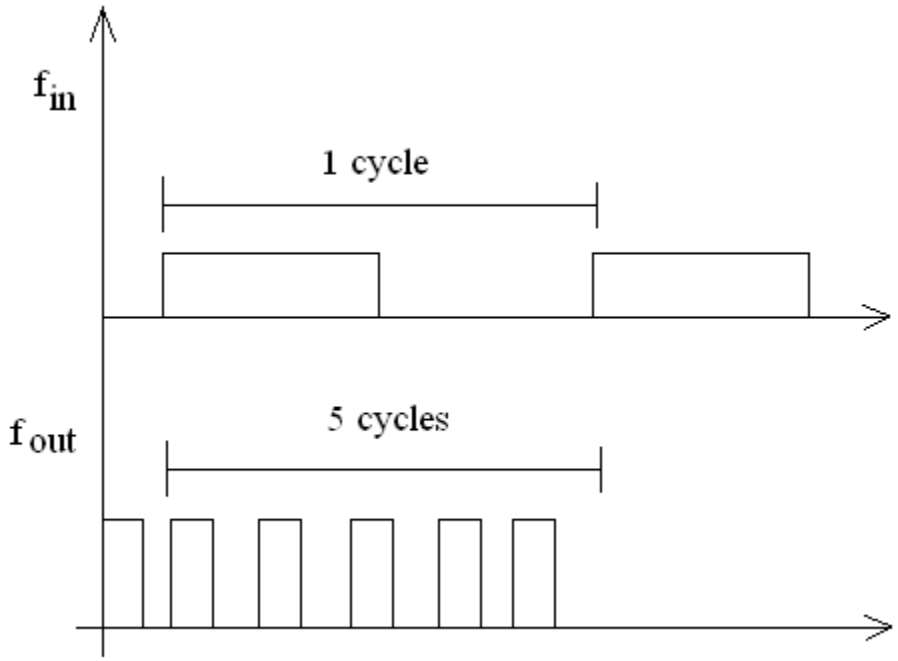
```
% program for frequency synthesizer
close all;
clear all;
clc
fs = 10000;
t = 0:1/fs:1.5;
f=50;
```

```
x1 = square(2*pi*f*t);
subplot(3,1,1)
plot(t,x1); axis([0 0.2 -1.2 1.2])
xlabel('Time (sec)');ylabel('Amplitude');
title('Square wave input with freq=50HZ');
t = 0:1/fs:1.5;
x2 = square(2*pi*2*f*t);
subplot(3,1,2)
plot(t,x2); axis([0 0.2 -1.2 1.2])
xlabel('Time (sec)');ylabel('Amplitude');
title('frequency multiplication by a factor of 2');
x3 = square(2*pi*f/2*t);
subplot(3,1,3)
plot(t,x3); axis([0 0.2 -1.2 1.2])
xlabel('Time (sec)');ylabel('Amplitude');
title('frequency division by a factor of 2');
```

PROCEDURE:

1. Switch on the trainer and verify the output of the regulated power supply i.e. $\pm$ 5V. These supplies are internally connected to the circuit so no extra connections are required.
2. Observe output of the square wave generator using oscilloscope and measure the range with the help of frequency counter, frequency range should be around 1 KHz to 10 KHz.
3. Calculate the free running frequency range of the circuit (VCO output between 4^{th} pin and ground). For different values of timing resistor R1 (to measure R_t switch off the trainer and measure R_t value using digital multimeter between given test points) . and record the frequency values in tabular 1. $F_{out} = 0.3 /(R_tC_t)$ where R_t is the timing resistor and C_t is the timing capacitor =0.01 µf.
4. Connect 4^{th} pin of LM 565 (F_{out}) to the driver stage and 5^{th} pin (Phase comparator) connected to 11^{th} pin of 7490. Output can be taken at the 11^{th} pin of the 7490. It should be divided by the 10, 2 times of the f_{out}.

EXPECTED WAVEFORMS:



F_{in} KHz	$F_{out} = N f_{in}$ KHz	Divided by 10,2

RESULT:

QUESTIONS:

1. What are the applications of PLL?
2. What is PLL?
3. Define Lock range of a PLL?
4. What is a VCO?
5. What are the applications of frequency synthesizer?
6. What is meant by the free running frequency of PLL?
7. What is the operation of a frequency synthesizer?
8. Which block is mainly used in frequency synthesizer?

EXPERIMENT NO-14 DATE:

AGC CHARADTERISTICS

AIM: To study the operation of AGC in communication system.

APPARATUS:

1. Trainer Kit
2. Dual trace oscilloscope
3. Digital multi meter.
4. PC with windows(95/98/XP/NT/2000)
5. MATLAB Software with communication toolbox

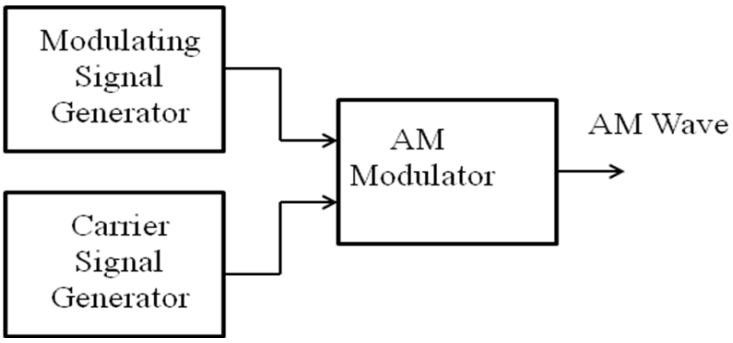
THEORY:

A Simple AGC is a system by means of which the overall gain of a radio receiver is varied automatically with the changing strength of the received signal, to keep the output substantially constant. A dc bias voltage, derived from the detector. The devices used in those stages are ones who's trans-conductance and hence gain depends on the applied bias voltage or current. It may be noted in passing that, for correct AGC operation, this relationship between applied bias and trans-conductance need not to be strictly linear, as long as trans-conductance drops significantly with increased bias.

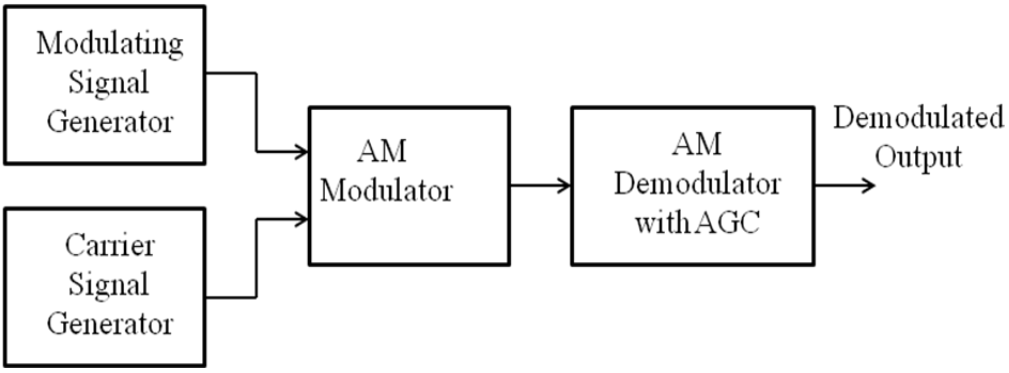
All modern receivers are furnished with AGC, which enables tuning to stations of varying signal strengths without appreciable change in the size of the output signal thus AGC "irons out" input signal amplitude variations, and the gain control dose not have to be re adjusted every time the receiver is tuned from one station to another, except when the change in signal strengths is enormous. In addition, AGC helps to smooth out the rapid fading which may occur with long-distance short-wave reception and prevents the overloading of last IF amplifier which might otherwise have occurred.

BLOCK DIAGRAM:

AM Modulator:



Demodulator:



PROGRAM:

```
% program for AGC
close all
clear all
clc
Fs = 100e3;     %sampling freq
t = 0:1/Fs:.1-1/Fs;              % time variable
Am=2;
fm = 100;  %fm 100 Hz
m = cos(2*pi*fm*t);     %message signal
Fc = 0.5e3;
% am modulation
 Ac = 8;
c=Ac.*cos(2*pi*Fc*t);   %carrier signal
```

```
figure;
% ploting message and carrier signals
subplot(2,1,1);
plot(c);
title('carrier');xlabel('time');ylabel('amplitude');
subplot(2,1,2);
plot(m);
title('message');xlabel('time');ylabel('amplitude');
figure;
% ploting AM modulated output
s = ammod(m,Fc,Fs,0,Ac);
subplot(2,1,1);
plot(s);
title('am modulation ');xlabel('time');ylabel('amplitude');
z = amdemod(s,Fc,Fs,0,Ac);
subplot(2,1,2);
plot(z);
title('am demodulation ');xlabel('time');ylabel('amplitude');
```

PROCEDURE:

1. As the circuit is already wired you just have to trace the circuit according to the Circuit diagram given above Fig1.1.
2. Connect the trainer to the mains and switch on the power supply.
3. Measures the output voltages of the regulated power supply circuit i.e. +12v and -12v,+6@150ma.
4. Observe outputs of RF and AF signal generator using CRO, note that RF voltage is approximately 50mVpp of 455KHz frequency and AF voltage is 5Vpp of 1KHZ frequency.
5. Now vary the amplitude of AF signal and observe the AM wave at output, note the Percentage of modulation for different value of AF signal.

$$\%\text{Modulation} = (B-A)/(B+A) \times 100$$

6. Now adjust the modulation index to 30% by varying the amplitudes of RF & AF Signals simultaneously.

7. Connect AM output to the input of AGC and also to the CRO channel-1.

8. Connect AGC link to the feedback network through OA79 diode

9. Now connect CRO channel-2 at output. The detected audio signal of1 KHz will be observed.

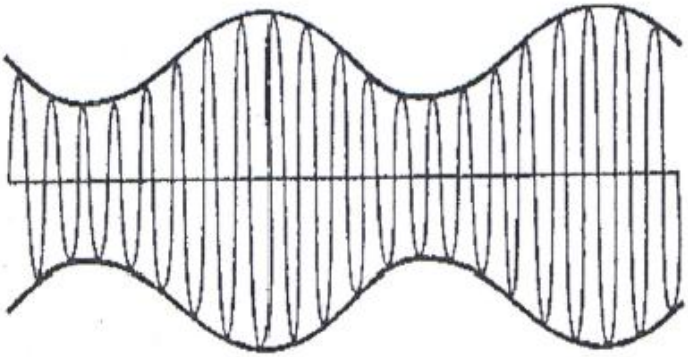
10. Calculate the voltage gain by measuring the amplitude of output signal (Vo) waveform, using formula A = Vo/Vi.

11. Now vary input level of 455 KHz IF signal and observe detected 1 KHz audio Signal with and without AGC link. The output will be distorted when AGC link removed i.e. there is no AGC action.

12. This explains AGC effect in Radio circuit.

EXPECTED WAVEFORMS:

.: AF Modulated RF Input.



: Detected Output With AGC:

RESULT:

QUESTIONS

1. What is the need for AGC in communications receivers?
2. Mention different types of AGC and suggest the best one ?

EXPERIMENT.NO-15 DATE:

PLL AS FM DEMODULATOR

AIM: To study the characteristics of PLL and calculate its capture range, lock range and free running VCO frequency.

APPARATUS:

1. PLL Trainer Kit
2. C R O (20MHz)
3. Digital Multimeter
4. PC with windows(95/98/XP/NT/2000)
5. MATLAB Software with communication toolbox

THEORY:

Phase Locked Loop is a versatile electronic servo system that compares the phase and frequency of a given signal with an internally generated reference signal. It is used in various applications like frequency multiplication, FM detector, AM modulator & De modulator and FSK etc.,

Free running frequency (f_0):

When there is no input signal applied to pin no:2 of PLL,it is in free running mode and the free running frequency is determined by the circuit elements R_t and C_t and is given by

$F_0 = 0.3/(R_tC_t)$ where R_t is the timing resistor

C_t is the timing capacitor

Lock range of PLL (f_L):

Lock range of PLL is in the range of frequencies in which PLL will remain lock, and this is given by

$f_L = \pm 8f_0 / V_{CC}$ Where f_0 is the free running frequency

$V_{CC} = V_{CC} - (- V_{CC})$

$= 2 V_{CC}$

Capture range(f_C):

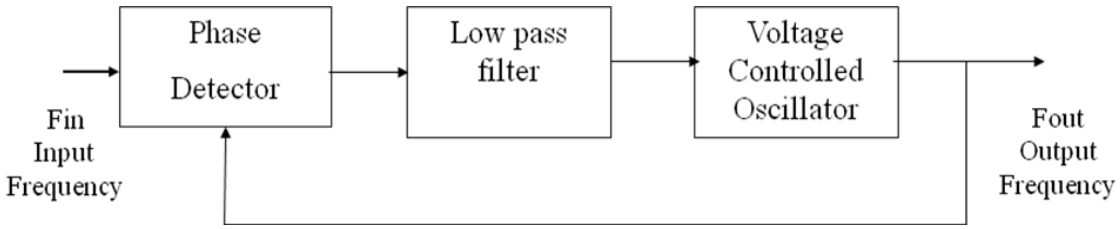
The capture range of PLL is the range of frequencies over which PLL acquires the lock. This is given by

$$f_C = \frac{1}{2\Pi}\sqrt{\frac{2\Pi f_L}{3.6x10^3 xC_C}}$$ Where f_L is the lock range and

C_C is filter capacitor

$R = 3.6 \text{ X } 10^3$

PLL BLOCK DIAGRAM:



PROGRAM:

```
close all;
clear all;
reg1 =0;
reg2 =0;
reg3 = 0;
eta =sqrt(2)/2;
theta =2*pi*1/100;
Kp = [(4*eta*theta)/(1+2*eta*theta+theta^2)];
Ki = [(4*theta^2)/(1+2*eta*theta+theta^2)];
d_phi_1 = 1/20;
n_data = 100;
for nn =1:n_data
phi1= reg1 +d_phi_1;
phi1_reg(nn) = phi1;
s1 =exp(j*2*pi*reg1);
s2 =exp(j*2*pi*reg2);
s1_reg(nn) =s1;
s2_reg(nn) =s2;
t =s1*conj(s2);
```

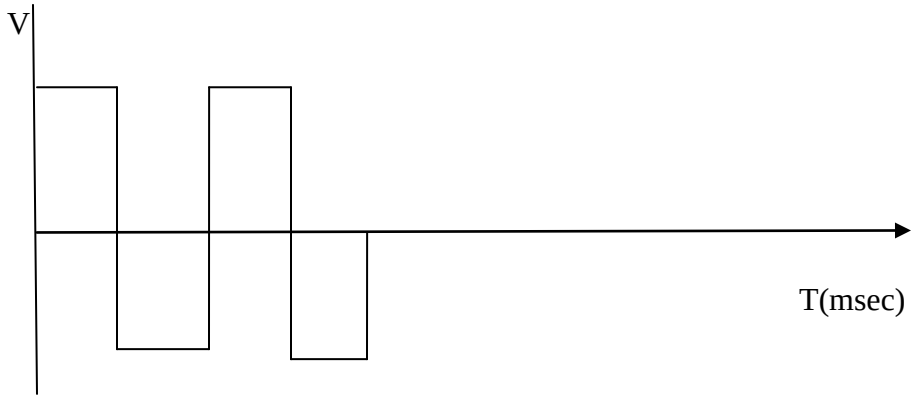
```
phi_error =atan(imag(t)/real(t))/(2*pi);
phi_error_reg(nn) = phi_error;
sum1 =Kp*phi_error + phi_error*Ki+reg3;
reg1_reg(nn) =reg1;
reg2_reg(nn) = reg2;
reg1 =phi1;
reg2=reg2+sum1;
reg3 =reg3+phi_error*Ki;
phi2_reg(nn) =reg2;
end
figure(1)
plot(phi1_reg);
hold on
plot(phi2_reg,'r');
hold off;
grid on;
title('phase plot');
xlabel('Samples');
ylabel('Phase');
figure(2)
plot(phi_error_reg);
title('phase Error of phase detector');
grid on;
xlabel('samples(n)');
ylabel('Phase error(degrees)');
figure(3)
plot(real(s1_reg));
hold on;
plot(real(s2_reg),'r');
hold off;
grid on;
```

```
title('Input signal & Output signal of VCO');
xlabel('Samples');
ylabel('Amplitude');
axis([0 n_data -1.1 1.1]);
```

OBSERVATIONS:

Theoritical values	Practical values
1.free running frequency	
Fo=1.2/4R1C1	
2.Lock in Frequency range	

EXPECTED WAVEFORM:



PROCEDURE:

1. Switch ON the experimental board by connecting the power card to the AC mains.
2. Then check the VCO output at pin 4.
3. This is a square waveform. The frequency of the wave from depends on C_T (0.01 μf) and R_5 (variable 10KΩ potentiometer).
4. Next Short pin 4 and pin 5. and give any signal of variable frequency and observe VCO output.
5. Change the input frequency and observe the VCO output on the CRO.

6. Between some frequencies, the VCO output is locked to the input signal frequency. This can be observed by increasing of decreasing the frequency of the VCO output by changing input frequency.
7. Before or after that frequency range, VCO output is not locked.
8. By changing the potentiometer provided on the board, locking frequency range can be changed.

RESULT:

QUESTIONS

1.What are the applications of PLL?

2.What is a PLL?

3.What is a VCO?

4.Define the lock range of a PLL?

5.Define the capture range of PLL?

6.Give the expression for free running frequency f_0 of a PLL?

7.What is meant by the free running frequency of a PLL?

8. Give the formulae for the lock range and capture range of the PLL?

ICA & HDL SIMULATION

LABORATORY MANUAL

III – I SEMESTER

Prepared By

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Mrs. P.Anitha, **Associate Professor**

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGG

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

(Sponsored by CMR Educational Society)

(Affiliated to JNTU, Hyderabad)

Secunderabad-14.

CONTENTS

CYCLE-I

CYCLE-II

VISION

To evolve into a center of excellence in Engineering Technology through creative and innovative practices in teaching-learning, promoting academic achievement & research excellence to produce internationally accepted competitive and world class professionals.

MISSION

To provide high quality academic programmes, training activities, research facilities and opportunities supported by continuous industry institute interaction aimed at employability, entrepreneurship, leadership and research aptitude among students.

QUALITY POLICY

- Impart up-to-date knowledge to the students in Electronics & Communication area to make them quality engineers.
- Make the students experience the applications on quality equipment and tools.
- Provide systems, resources and training opportunities to achieve continuous improvement.
- Maintain global standards in education, training and services.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: PROFESSIONALISM & CITIZENSHIP To create and sustain a community of learning in which students acquire knowledge and learn to apply it professionally with due consideration for ethical, ecological and economic issues.
PEO2: TECHNICAL ACCOMPLISHMENTS To provide knowledge based services to satisfy the needs of society and the industry by providing hands on experience in various technologies in core field.
PEO3: INVENTION, INNOVATION AND CREATIVITY To make the students to design, experiment, analyze, interpret in the core field with the help of other multi disciplinary concepts wherever applicable.
PEO4: PROFESSIONAL DEVELOPMENT To educate the students to disseminate research findings with good soft skills and become a successful entrepreneur.
PEO5: HUMAN RESOURCE DEVELOPMENT To graduate the students in building national capabilities in technology, education and research.

CODE OF CONDUCT FOR THE LABORATORIES

- All students must observe the Dress Code while in the laboratory.
- Sandals or open-toed shoes are NOT allowed.
- Foods, drinks and smoking are NOT allowed.
- All bags must be left at the indicated place.
- The lab timetable must be strictly followed.
- Be PUNCTUAL for your laboratory session.
- Program must be executed within the given time.
- Noise must be kept to a minimum.
- Workspace must be kept clean and tidy at all time.
- Handle the systems and interfacing kits with care.
- All students are liable for any damage to the accessories due to their own negligence.
- All interfacing kits connecting cables must be RETURNED if you taken from the lab supervisor.
- Students are strictly PROHIBITED from taking out any items from the laboratory.
- Students are NOT allowed to work alone in the laboratory without the Lab Supervisor
- USB Ports have been disabled if you want to use USB drive consult lab supervisor.
- Report immediately to the Lab Supervisor if any malfunction of the accessories, is there.

Before leaving the lab

- Place the chairs properly.
- Turn off the system properly
- Turn off the monitor.
- Please check the laboratory notice board regularly for updates.

CYCLE - I

INTRODUCTION

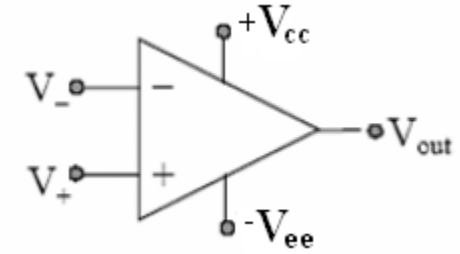
STUDY OF IC741, IC555 & IC565

AIM: To study pin details, specifications, applications and features of IC741 (Op-Amp) IC555 (Timer) & IC565.

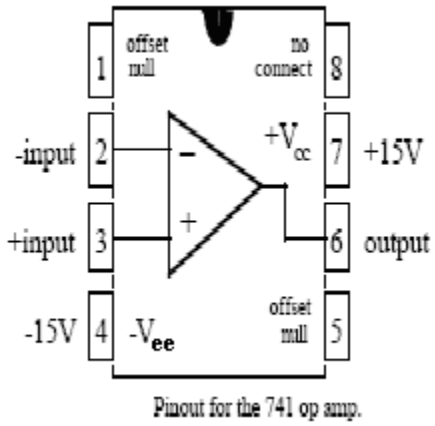
COMPONENTS: IC741, IC555 & IC565

IC741: (Operational Amplifier)

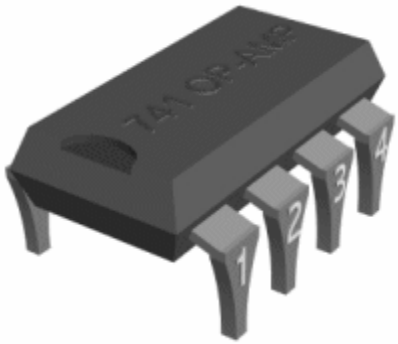
Symbol:



Pin Configuration:



Pinout for the 741 op amp.



Specifications:

Supply Voltage	**± 18V**
Internal Power Dissipation	310mw
Differential input voltage	± 30V
Input Voltage	**± 15V**
Operating temperature range	0ºC to 70ºC

Applications:

Non-inverting amplifier
Inverting amplifier
Integrator

Differentiator
Low Pass, High Pass, Band pass and Band Reject Filters

Features:

No External frequency compensation is required
Short circuit Protection
Off Set Null Capability
Large Common mode and differential Voltage ranges
Low Power Dissipation

No-Latch up Problem
741 is available in three packages: 8-pin metal can, 10-pin flat pack and 8 or 14-pin DIP

IC555: (Timer)

Pin Configuration:

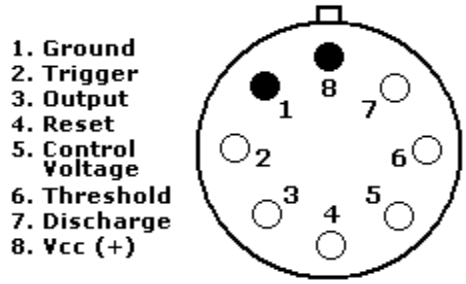


fig. 1. 8-pin T package

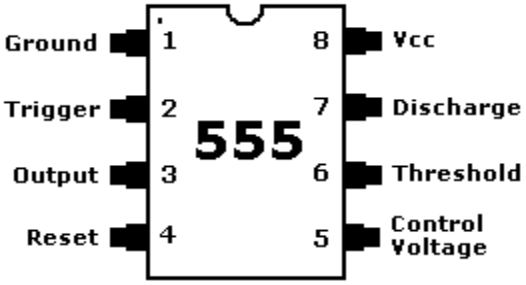
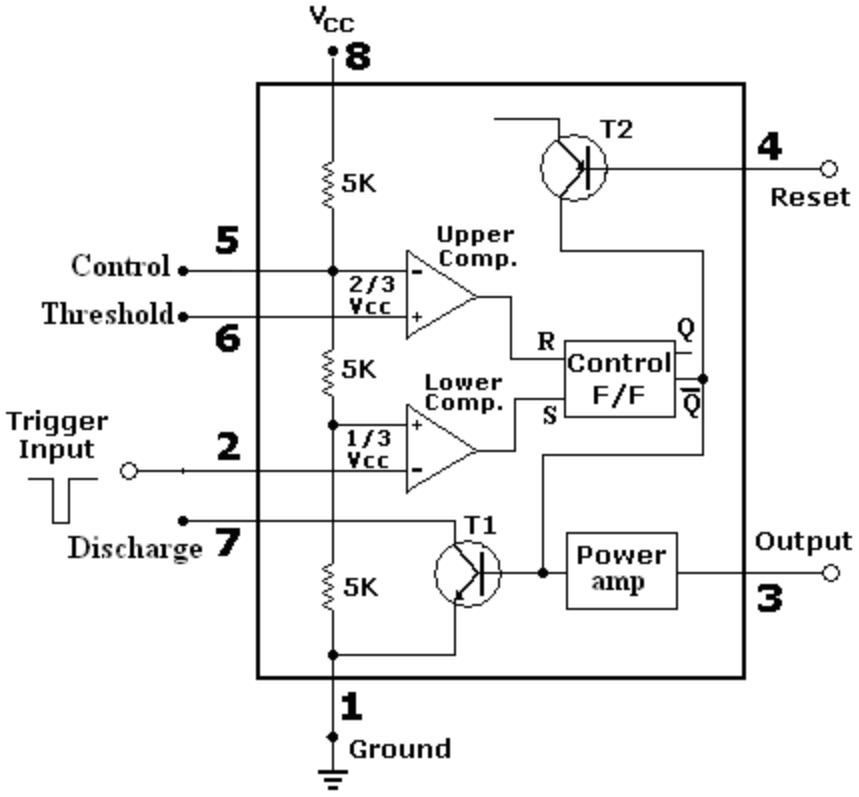


fig. 2. 8-pin V package

Functional block diagram:



Specifications:

Supply Voltage 5V to 18V

Maximum Current rating 200mA

Minimum Triggering Voltage - (1/3) VCC

Operating temperature range 0ºC to 70ºC

Applications:

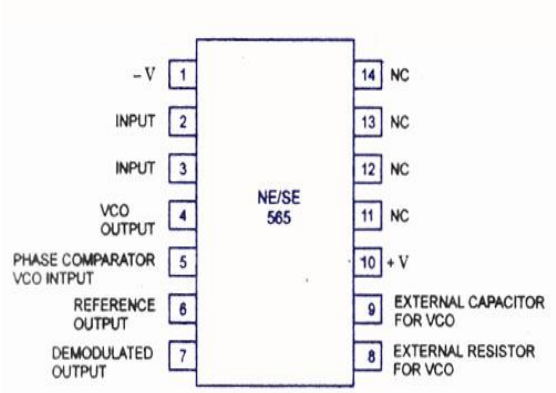
1. Astable Multivibrator, Schmitt trigger, Free running ramp Generator, etc.,
2. Monostable Multivibrator, Frequency divider, Pulse structure

Features:

555 timers are reliable, easy to use and low cost. The device is available as an 8 pin circular style, an 8–pin mini DIP or a 14 Pin DIP

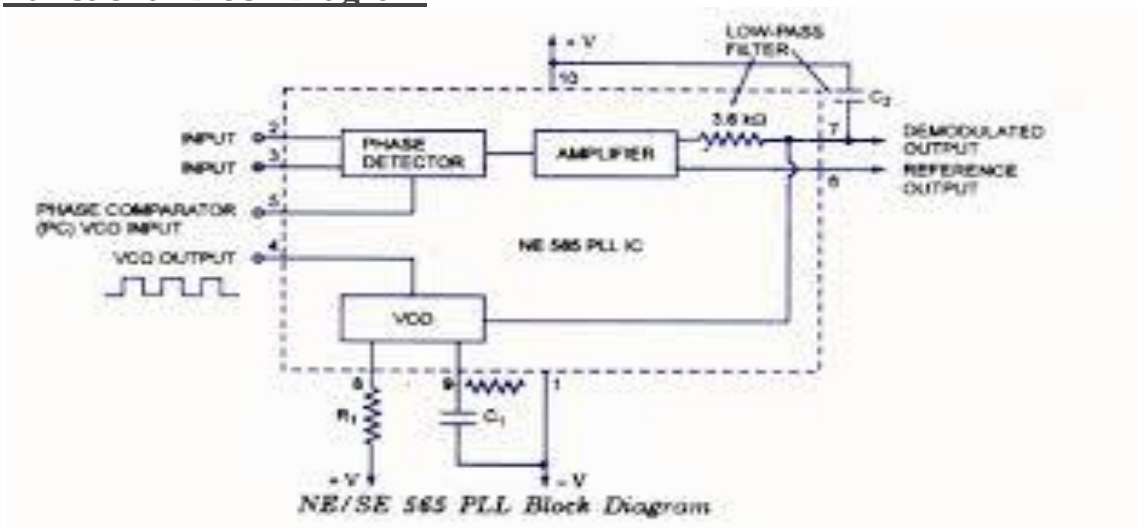
IC565: Phase Locked Loop (PLL)

Pin Configuration



14-Pin DIP Package

Functional Block Diagram



NE/SE 565 PLL Block Diagram

Monolithic PLL Characteristics

- Operating frequency range: 0.001 Hz to 500 kHz.
- Operating voltage range: ± 6 to ± 12 V.
- Input impedance: 10 k Q typically.
- Output sink current: 1mA typically.
- Output source current: 10 m A typically.
- Drift in VCO centre frequency with temperature: 300 ppm/ °C typically.
- Drift in VCO centre frequency with supply voltage: 1.5 %/V maximum.
- Input level required for tracking: 10 mVrms minimum to 3 V peak-to-peak maximum.
- Bandwidth adjustment range: < ± 1 to > ± 60 %.

Applications:

1. Modems
2. FSK Demodulation
3. FM Demodulation
4. Frequency Synthasizers etc.

QUESTIONS:

1. What is the symbol of op-amp?
2. Draw the pin diagram of op-amp.
3. What is the supply voltage range that an op-amp can with stand?
4. What is the input voltage range that an op-amp can with stand?
5. What are the available package types of IC741?
6. What is a virtual ground? What are the differences between the physical ground and the virtual ground?
7. What is the current flowing through the input terminals of an Ideal op-amp?
8. Which loop voltage gain is larger, closed or open?
9. What is the normal value of saturation voltage of an op-amp?
10. Mention a few applications of op-amp.
11. Mention some features of op-amp.
12. What is the main purpose of IC555 timer?
13. Draw the pin diagram of op-amp.
14. Draw the functional diagram of IC555 timer.
15. How many comparators are present in IC555 timer?
16. What are the trigger voltages of UC and LC?
17. What is the functionality of power amplifier in the output stage of IC555 timer?
18. Which is the Flip-Flop used in IC555 timer?
19. What is the use of RESET pin in IC555 timer?
20. What are the available package types of IC555 timer?
21. Mention a few applications of IC555 timer.
22. What is the dc level required for the negative going trigger pulse at pin 2 of IC555 timer?
23. What is IC565?
24. Draw the pin diagram of IC565

EXPERIMENT NO: 1 **DATE:**

OP-AMP APPLICATIONS - ADDER, SUBTRACTOR & COMPARATOR

AIM: To study Adder, Subtractor & Comparator circuits using OP-AMP IC741 and verify their theoretical and practical output.

APPARATUS:
Bread Board
IC741, Resistors
DC Supply
Function Generator
Multi meter
CRO
Probes, Connecting Wires

THEORY:

Adder: Op-amp can be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or an adder. Summing amplifier can be classified as inverting & non-inverting summer depending on the input applied to inverting & non-inverting terminals respectively. Circuit Diagram shows a non-inverting adder with n inputs. Here the output will be the linear summation of input voltages. The circuit can be used either as summing amplifier, scaling amplifier, or as averaging amplifier.

From the circuit of adder, it can be noted that at pin3

$$I_1+I_2+I_3+\ldots\ldots\ldots\ldots I_n=0$$

$$\frac{\quad}{\quad}+\frac{\quad}{\quad}+\frac{\quad}{\quad}+\ldots\ldots\ldots\ldots\frac{\quad}{\quad}=0$$

$$\frac{\quad}{\quad}=0$$

$$V_a=\frac{\quad}{\quad}$$

$$V_o \quad — \quad Va$$

$$V_o \quad — \quad (\frac{\quad}{\quad})$$

$$V_o = (1+\frac{\quad}{\quad})\ (\frac{\quad}{\quad})$$

$$= (1+ (n-1)) \left(\frac{R_f}{R_1}\right)$$

$$= n \left(\frac{R_f}{R_1}\right)$$

$$\mathbf{V_o = V_1+V_2+V_3+\ldots+V_n}$$

This means that the output voltage is equal to the sum of all the input voltages.

Subtractor: A subtractor is a circuit that gives the difference of the two inputs, $V_o = V_2 - V_1$, Where V_1 and V_2 are the inputs. By connecting one input voltage V_1 to inverting terminal and another input voltage V_2 to the non – inverting terminal, we get the resulting circuit as the Subtractor. This is also called as differential or difference amplifier using op-amps.
Output of a differential amplifier (subtractor) is given as

$$V_o = (-R_f/R_1)(V_1 - V_2)$$

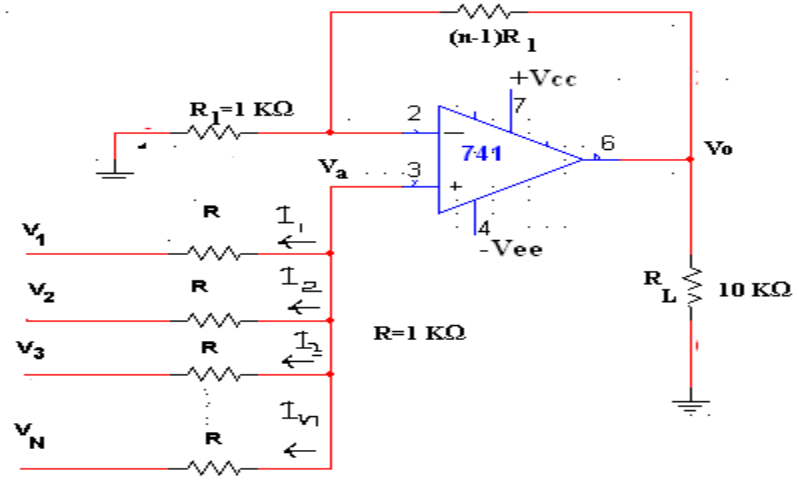
If all external resistors are equal in value, then the gain of the amplifier is equal to -1. The output voltage of the differential amplifier with a gain of -1 is

$$V_o = (V_2 - V_1)$$

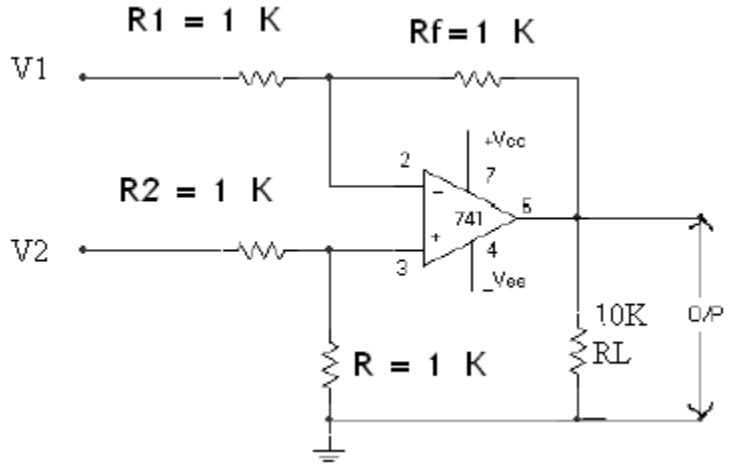
Thus the output voltage V_o is equal to the voltage V_2 applied to the non – inverting terminal minus the voltage V_1 applied to the inverting terminal. Hence the circuit is called a Subtractor.

Comparator: A Comparator is a non-linear signal processor. It is an open loop mode application of Op-amp operated in saturation mode. Comparator compares a signal voltage at one input with a reference voltage at the other input. Here the Op-amp is operated in open loop mode and hence the output is $\pm V_{sat}$. It is basically classified as inverting and non-inverting comparator. In a non-inverting comparator V_{in} is given to +ve terminal and V_{ref} to –ve terminal. When $V_{in} < V_{ref}$, the output is $-V_{sat}$ and when $V_{in} > V_{ref}$, the output is $+V_{sat}$ (see expected waveforms). In an inverting comparator input is given to the inverting terminal and reference voltage is given to the non inverting terminal. The output of the inverting comparator is the inverse of the output of non-inverting comparator. The comparator can be used as a zero crossing detector, window detector, time marker generator and phase meter.

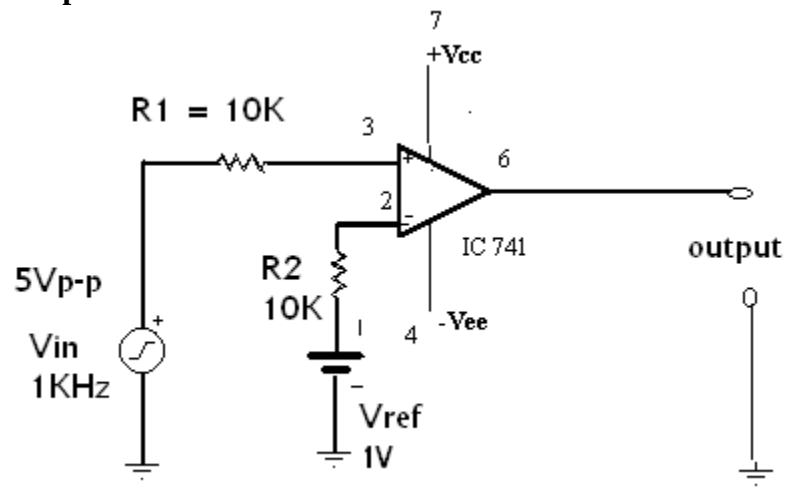
CIRCUIT DIAGRAM:
Adder:



Subtractor:



Comparator:



PROCEDURE:

Adder:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply dc voltages at each input terminal for V_1 and V_2 from the dc supply and check the output voltage V_o at the output terminal.
4. Tabulate 3 different sets of readings by repeating the above step.
5. Compare practical V_o with the theoretical output voltage $V_o = V_1 + V_2$.

Subtractor:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply dc voltages at each input terminal for V_1 and V_2 from the dc supply and check the output voltage V_o at the output terminal.
4. Tabulate 3 different sets of readings by repeating the above step.
5. Compare practical V_o with the theoretical output voltage $V_o = V_2 - V_1$.

Comparator:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply 1 KHz sine wave with 5 V_{pp} at the non-inverting input terminal of IC741 using a function generator.
4. Apply 1V dc voltage as reference voltage at the inverting terminal of IC741.
5. Connect the channel-1 of CRO at the input terminals and channel-2 of CRO at the output terminals.
6. Observe the input sinusoidal signal at channel-1 and the corresponding output square wave at channel-2 of CRO. Note down their amplitude and time period.
7. Overlap both the input and output waves and note down voltages at positions on sine wave where the output changes its state. These voltages denote the Reference voltage.
8. Plot the output square wave corresponding to the sine input with V_{ref} = 1V.

TABLE:

Adder:

S.No.	V_1 Volts	V_2 Volts	Theoretical $V_o=V_1+V_2$	Practical V_o Volts

Subtractor:

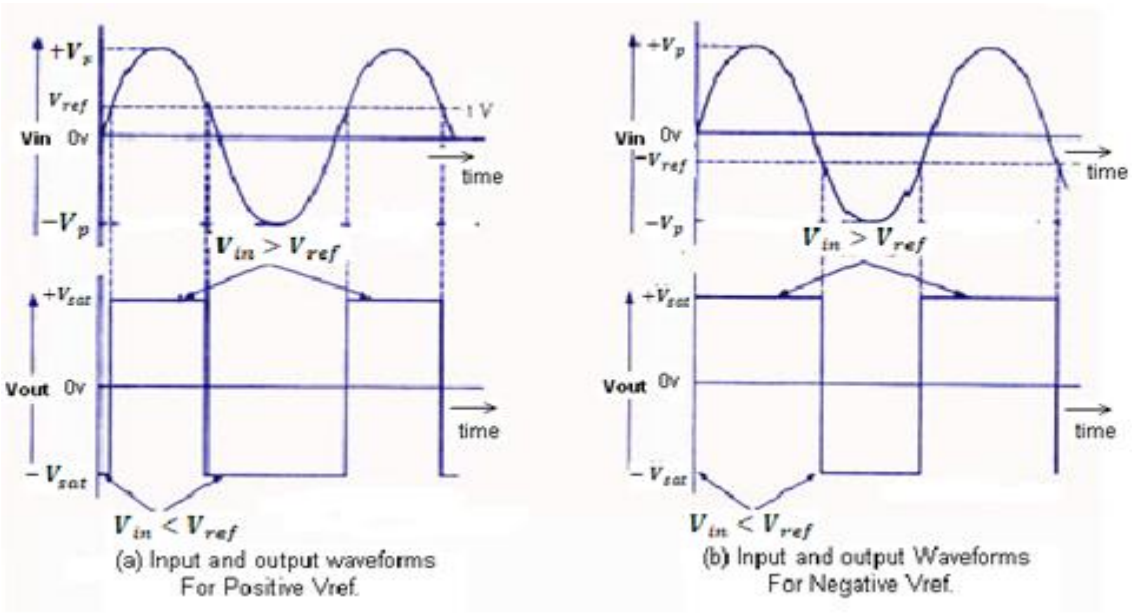
S.No.	V_1 Volts	V_2 Volts	Theoretical $V_o=V_2-V_1$	Practical V_o Volts

Comparator:

Theoretical Reference voltage (from circuit)	
Practical Reference voltage (from output waveforms)	

EXPECTED WAVEFORMS:

COMPARATOR INPUT & OUTPUT WAVEFORMS



RESULT:

QUESTIONS:

1. Draw the circuit diagram of 3 input adder.
2. What is the other name for adder?
3. Draw the circuit diagram of a Subtractor.
4. Which amplifier acts as a Subtractor?
5. How many basic input parameters are required for a comparator?
6. Draw the circuit diagram of a non-inverting comparator and inverting comparator.
7. What is the output of a non-inverting comparator and inverting comparator if the input is sinusoidal?
8. What are the differences between the Inverting and Non–Inverting comparator?
9. What is the name of the comparator if the reference voltage is 0V?
10. Draw the circuit diagram and the output waveform of a Zero Crossing Detector if the input is sinusoidal?
11. What is the name of a regenerative comparator?
12. Draw an op- amp circuit whose output V_o is $V_1 + V_2 - V_3 - V_4$.

XPERIMENT NO: 2 **DATE:**

INTEGRATOR AND DIFFERENTIATOR USING IC741 OP-AMP

AIM: To study the operation of the Integrator & differentiator using op-amp and trace the output wave forms for sine and square wave inputs.

APPARATUS: Bread Board
IC741, Resistors, Capacitors
Function Generator
CRO
Probes
Connecting wires

THEORY:

Integrator:

A circuit in which the output voltage is the integration of the input voltage is called an integrator**.**

$$V_o = -\frac{1}{R_1 C_f} \int V_{in}\, dt \qquad \text{(1)}$$

In the practical integrator to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F. Thus, R_F limits the low-frequency gain and hence minimizes the variations in the output voltage.

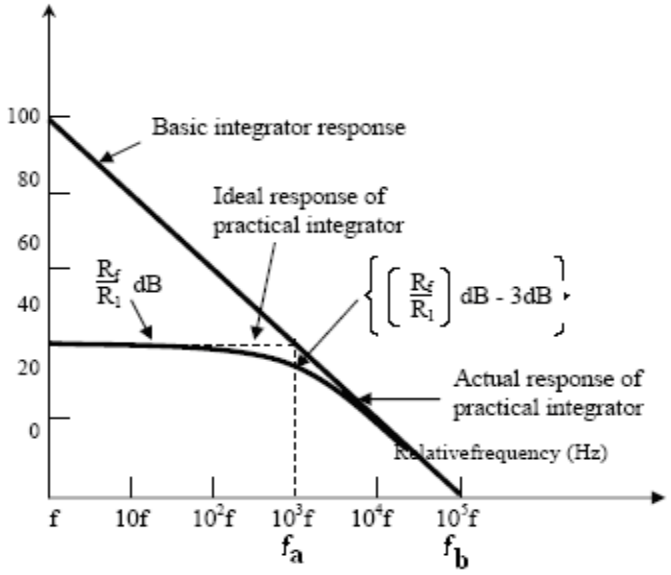


Fig 2.1 Frequency Response of Integrator

The frequency response of the integrator is shown in the fig. 2.1. f_b is the frequency at which the gain is 0 dB and is given by

$$f_b = 1/2\pi R_1 C_f.$$

In this fig. there is some relative operating frequency, and for frequencies from f to f_a the gain R_F/R_1 is constant. However, after f_a the gain decreases at a rate of 20 dB/decade. In other words, between f_a and f_b the circuit of fig. 2.1 acts as an integrator. The gain-limiting frequency f_a is given by

$$f_a = 1/2\pi R_f C_f.$$

Normally $f_a<f_b$. From the above equation, we can calculate R_f by assuming f_a & C_f. This is very important frequency. It tells us where the useful integration range starts.

If $f_{in} < f_a$ - circuit acts like a simple inverting amplifier and no integration results,
If $f_{in} = f_a$ - integration takes place with only 50% accuracy results,
If $f_{in} = 10f_a$ - integration takes place with 99% accuracy results.

In the circuit diagram of Integrator, the values are calculated by assuming f_a as 50 Hz. Hence the input frequency is to be taken as 500Hz to get 99% accuracy results.

Integrator has wide applications in
1. Analog computers used for solving differential equations in simulation arrangements.
2. A/D Converters
3. Signal wave shaping
4. Function Generators.

Differentiator:

As the name suggests, the circuit performs the mathematical operation of differentiation, i.e. the output voltage is the derivative of the input voltage.

$$V_o = - R_f C_1 \frac{dV_{in}}{dt}$$

Both the stability and the high-frequency noise problems can be corrected by the addition of two components: R_1 and C_f, as shown in the circuit diagram. This circuit is a practical differentiator.

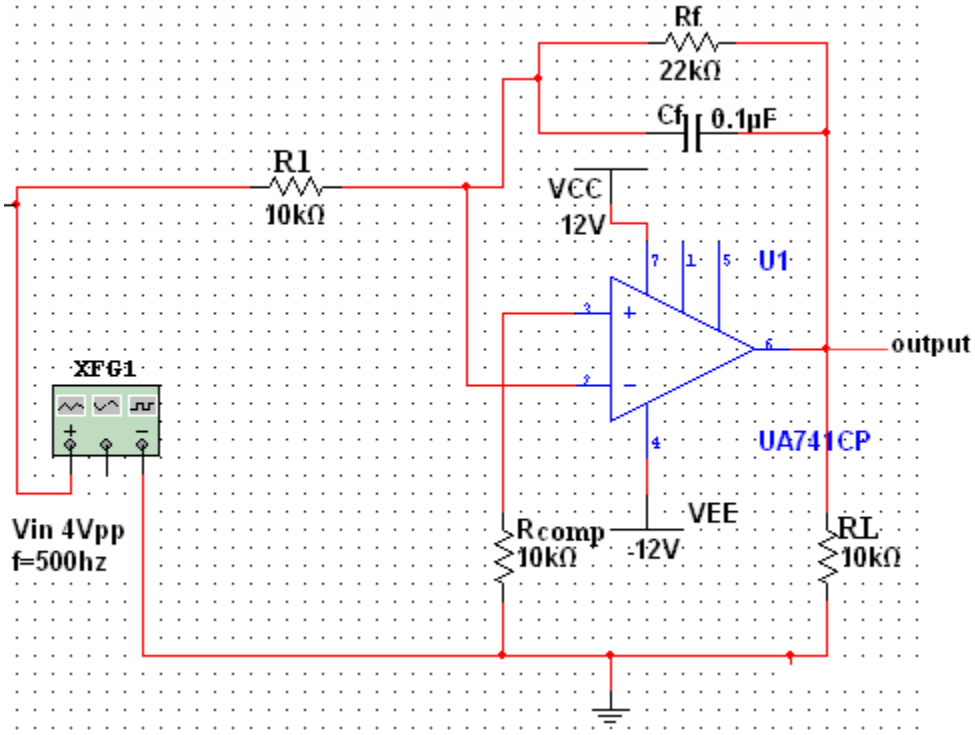
The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to R_fC_1. That is, $T>= R_fC_1$

Differentiator can be designed by implementing the following steps.
1. Select f_a equal to the highest frequency of the input signal to be differentiated.
Then, assuming a value of $C_1<1\ \mu F$, calculate the value of R_f
2. Calculate the values of $R_1$and C_f so that $R_1C_1=R_fC_f$.

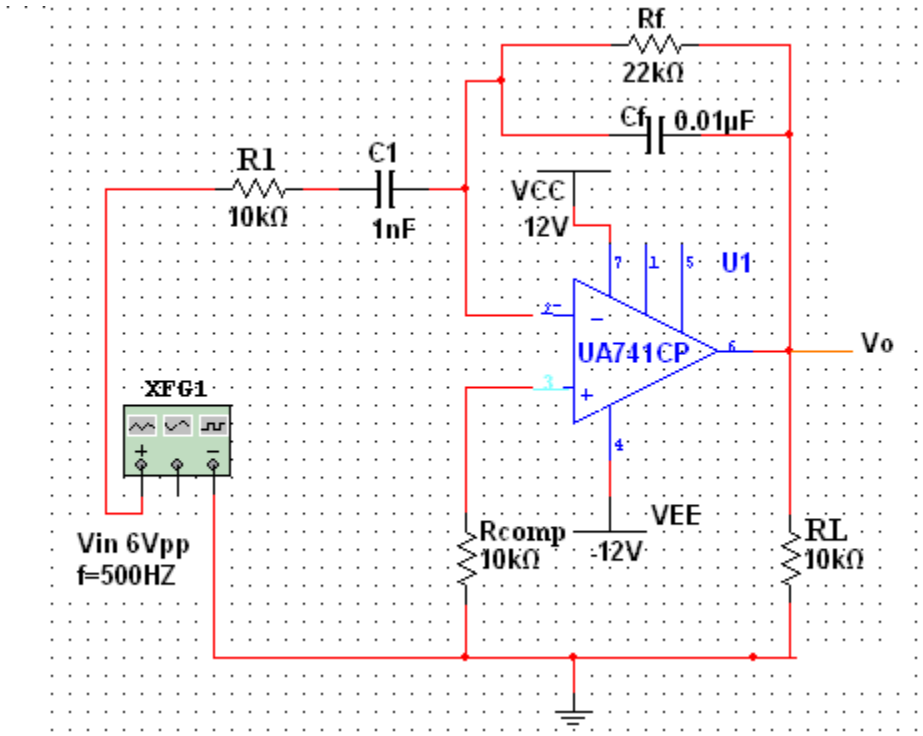
Differentiator has wide applications in
1. Monostable Multivibrator
2. Signal wave shaping
3. Function Generators.

CIRCUIT DIAGRAM:

Integrator:



Differentiator:



PROCEDURE:

Integrator:

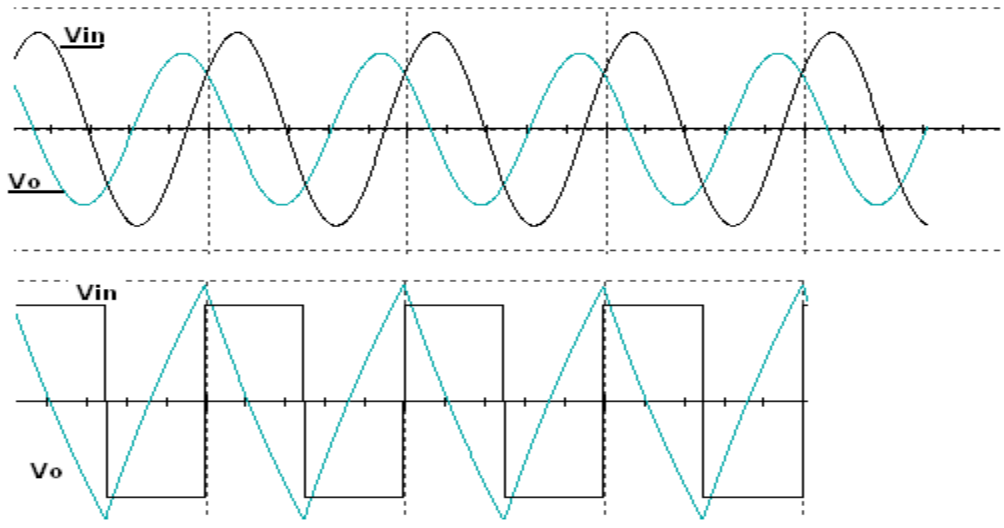
1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply sine wave at the input terminals of the circuit using function Generator.
4. Connect channel-1 of CRO at the input terminals and channel-2 at the output terminals.
5. Observe the output of the circuit on the CRO which is a cosine wave (90^o phase shifted from the sine wave input) and note down the position, the amplitude and the time period of V_{in} & V_o.
6. Now apply the square wave as input signal.
7. Observe the output of the circuit on the CRO which is a triangular wave and note down the position, the amplitude and the time period of V_{in} & V_o.
8. Plot the output voltages corresponding to sine and square wave inputs.

Differentiator:

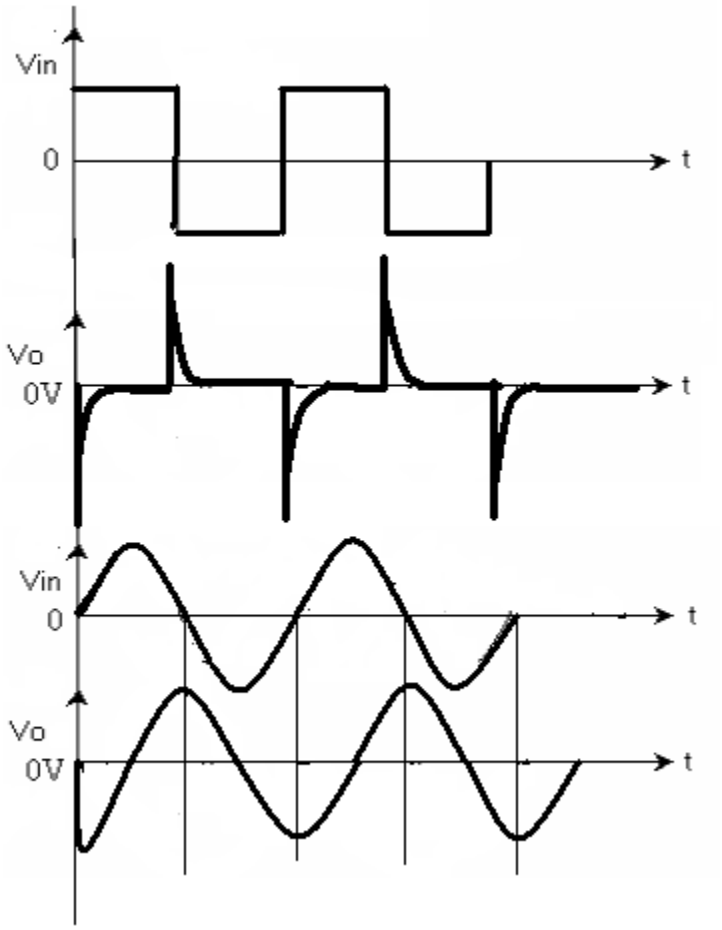
1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply sine wave at the input terminals of the circuit using function Generator.
4. Connect channel-1 of CRO at the input terminals and channel-2 at the output terminals.
5. Observe the output of the circuit on the CRO which is a cosine wave (90^o phase shifted from the sine wave input) and note down the position, the amplitude and the time period of V_{in} & V_o.
6. Now apply the square wave as input signal.
7. Observe the output of the circuit on the CRO which is a spike wave and note down the position, the amplitude and the time period of V_{in} & V_o.
8. Plot the output voltages corresponding to sine and square wave inputs.

EXPECTED WAVEFORMS:

Integrator



Differentiator:



RESULT:

QUESTIONS:

1. What is an Integrator?
2. Draw the circuit of the Integrator using op-amp IC741.
3. Write down the expression for V_o of an Integrator.
4. Draw the frequency response of the Integrator and explain.
5. Draw the output waveform of the Integrator when the input is a Square wave.
6. What is the purpose behind the connection of Rf in the feedback path of Integrator?
7. What are the applications of Integrator?
8. Why R_{comp} is used in both Integrator and Differentiator circuits?
9. What is a Differentiator?
10. Draw the circuit of the Differentiator using op-amp IC741.
11. Write down the expression for V_o of a Differentiator.
12. Draw the output waveform of the Differentiator when the input is a Sine wave.
13. Why R1 and Cf are connected in the circuit of the Differentiator?
14. What are the applications of Differentiator?

EXPERIMENT NO: 3 **DATE:**

ACTIVE FILTER APPLICATIONS - LPF & HPF (1ST ORDER)

a) 1st Order LOW PASS FILTER

AIM: To plot the frequency response of Butterworth LPF (First order) and find the high cut-off frequency.

APPARATUS: Bread Board
Function Generator
CRO
Probes
Connecting Wires
741 Op-amp, Resistors, Capacitors

THEORY:

Filters are classified as follows:

Based on components used in the circuit

- Active filters – Use active elements like transistor or op-amp(provides gain) in addition to passive elements
- Passive filters – Use only passive elements like resistors, capacitors and inductors, hence no gain here.

Based on frequency range

- Low pass filter(LPF) – Allows low frequencies
- High pass filter(HPF) – Allows high frequencies
- Band pass filter(BPF) – Allows band of frequencies
- Band reject filter(BRF) – Rejects band of frequencies

All pass filter – Allows all frequencies but with a phase shift

Active Filter is often a frequency – selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band.

These Active Filters are most extensively used in the field of communications and signal processing. They are employed in one form or another in almost all sophisticated electronic systems such as Radio, Television, Telephone, Radar, Space Satellites, and Bio-Medical Equipment.

Active Filters employ transistors or Op – Amps in addition to that of resistors and capacitors. Active filters have the following advantages over passive filters. (1) Flexible gain and frequency adjustment. (2) No loading problem (because of high input impedance and low output impedance) and (3) Active filters are more economical than passive filters.

A first – Order Low – Pass Butterworth filter uses RC network for filtering. Note that the op-amp is used in the non-inverting configuration; hence it does not load down the RC network. Resistors R_1 and R_F determine the gain of the filter.

The gain magnitude equation of the Low – Pass filter can be obtained by converting equation into its equivalent polar form, as follows.

$$| V_o / V_{in} | = A_F / \sqrt{1 + (f / f_H)^2}$$

Where $f_H = \frac{1}{2 \prod RC}$ = high cut-off frequency of the filter.

The operation of the low – pass filter can be verified from the gain magnitude equation.

1. At very low frequencies, that is $f < f_H$

   $| V_o/V_{in} | = A_F$

2. At $f = f_H$, $| V_o/V_{in} | = A_F/\sqrt{2} = 0.707\ A_F$

3. At $f > f_H$ $| V_o/V_{in} | < A_F$

Thus the Low – Pass filter has a constant gain A_F from 0 Hz to the almost high cut-off frequency, f_H, it has the gain $0.707A_F$ at exactly f_H, and after f_H it decreases at a constant rate with an increase in frequency. The gain decreases 20 dB (= 20 log 10) each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_H is 20 dB/decade. The frequency $f = f_H$ is called the cut-off frequency because the gain of the filter at this frequency is down by 3 dB (=20log 0.707) from 0 Hz. Other equivalent terms for cut-off frequency are -3dB frequency, break frequency, or corner frequency.

DESIGN:

1. Choose a value for high cut-off frequency, f_H(10 KHz) and a value for gain, A_F (2)
2. Assume a value of C≤1μF (3nF)
3. Calculate the value of R using the equation

---

4. Finally, select values of R_1 and R_F dependent on the desired pass band gain A_F using

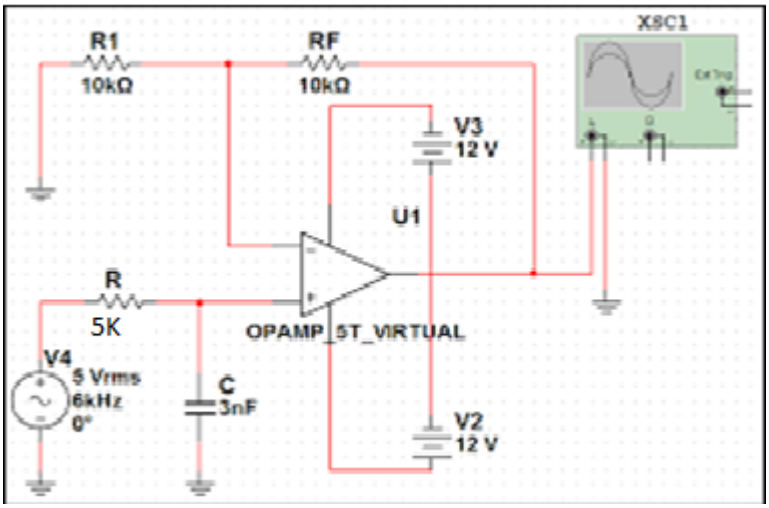
   $A_F = 1 + R_F/R_1$

   $2 = 1 + R_F/R_1$

   $R_F = R_1$

5. Assume a value for R_1 (10KΩ) and calculate R_F.

CIRCUIT DIAGRAM:



(You can assume any value for C which is available in the Lab)

PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.

3. Connect channel -1 of CRO to input terminals (V_{in}) and channel -2 to output terminals (V_o).
4. Set V_{in} = 5V & f_{in}=10Hz using function generator.
5. By varying the input frequency in regular intervals, note down the output voltage.
6. Calculate the gain (V_o/V_{in}) and Gain in dB = 20 log (V_o/V_{in}) at every frequency.
7. Plot the frequency response curve (taking frequency on X-axis & Gain in dB on Y-axis) using Semi log Graph.
8. Find out the high cut-off frequency, f_H (at Gain= Constant Gain, A_f – 3 dB) from the frequency response plotted.
9. Verify the practical (f_H from graph) and the calculated theoretical cut-off frequency (f_H = $1/2\pi RC$).

TABLE:

V_{in} = 5V

S.No.	Input Frequency f(Hz)	Output Voltage V_o (V)	Gain Magnitude $\lvert V_o/V_{in} \rvert$	Gain in dB = $20\log\lvert V_o/V_{in} \rvert$

CALCULATIONS:

THEORETICAL Cut-off frequency:

$f_H = 1 / (2\pi RC)$ = high cut-off frequency of the Low pass filter.

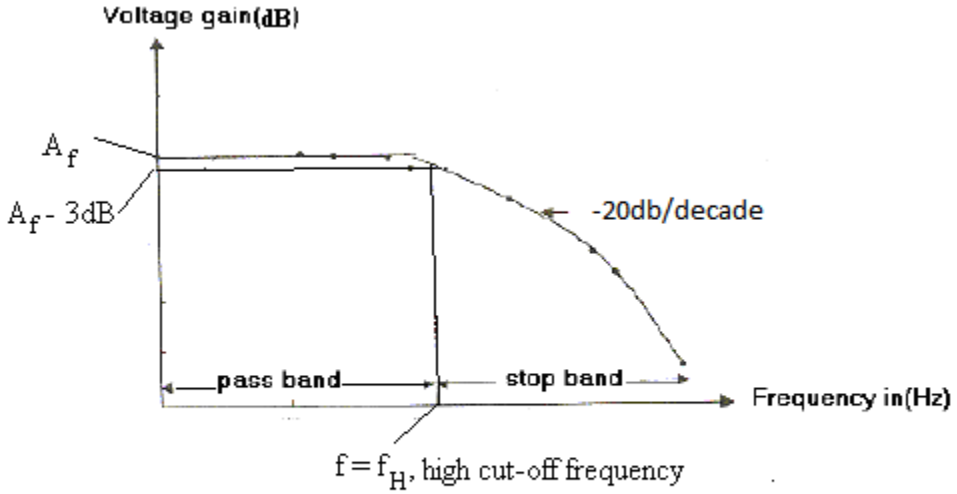
=

PRACTICAL Cut-off frequency (from Graph) :

f_H = high cut-off frequency of the Low pass filter

= 3dB cut-off frequency =

EXPECTED GRAPH:



RESULT:

ACTIVE LOW PASS & HIGH PASS BUTTERWORTH FILTERS (1st ORDER)

b) 1st Order HIGH PASS FILTER

AIM: To plot the frequency response of Butterworth HPF (First order) and find the low cut-off frequency.

APPARATUS: Bread Board
Function Generator
CRO
Probes
Connecting Wires
741 Op-amp, Resistors, Capacitors

THEORY:

First Order High Pass Filter consists of RC network for filtering. First Order High Pass filter can be constructed from a First Order Low Pass filter simply by interchanging frequency determining components R & C . Op-Amp is used in the non – inverting configuration. Resistor R_1 and R_F determine the gain of the Filter.

The voltage gain magnitude equation of the second order High-pass filter is

$$\left|\frac{V_0}{V_{in}}\right| = \frac{A_F\,(f/f_L)}{\sqrt{[1+(f/f_L)^2]}}$$

where $A_F = 1 + R_F / R_1$

f = Operating (input) frequency.

$f_L = \dfrac{1}{2\pi RC}$ = Low cut-off frequency of the filter.

This is the frequency at which the magnitude of the gain is 0.707 times its pass band value. Obviously, all frequencies higher than f_L are Pass Band frequencies, with the highest frequency determined by the closed-loop bandwidth of the OP-Amp.

The operation of the high–pass filter can be verified from the gain magnitude equation.

1. At very low frequencies, that is $f < f_L$
   $| V_o/V_{in} | < A_F$
2. At $f = f_L$, $| V_o/V_{in} | = A_F/\sqrt{2} = 0.707\ A_F$
3. At $f > f_L$, $| V_o/V_{in} | = A_F$

For example, in the first order High – Pass filter the gain rolls – off or increases at the rate of 20dB/decade in stop band, that is for input signal frequency lesser than Low cut-off frequency (f_L) ;

High Pass filter has constant gain A_F, after the Low cut-off frequency onwards (f_L).

DESIGN: Follow the same procedure as given for low-pass filter.

CIRCUIT DIAGRAM:

Take the circuit given in 1st Order LPF but interchange the places of Capacitor(C) and Resistor(R).

PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect channel -1 of CRO to input terminals (V_{in}) and channel -2 to output terminals (V_o).
4. Set V_{in} = 5V & f_{in}=10Hz using function generator.
5. By varying the input frequency in regular intervals, note down the output voltage.
6. Calculate the gain (V_o/V_{in}) and Gain in dB = 20 log(V_o/V_{in}) at every frequency.
7. Plot the frequency response curve (taking frequency on X-axis & Gain in dB on Y-axis) using Semi log Graph.
8. Find out the low cut-off frequency, f_L (at Gain= Constant Gain, A_f – 3 dB) from the frequency response plotted.
9. Verify the practical (f_L from graph) and the calculated theoretical cut-off frequency (f_L = $1/2\pi RC$).

TABLE:

V_{in} = 1V

S.No.	Input Frequency f(Hz)	Output Voltage V_o (V)	Gain Magnitude $\lvert V_o/V_{in} \rvert$	Gain in dB = $20\log\lvert V_o/V_{in} \rvert$

CALCULATIONS:

THEORETICAL Cut-off frequency:

$f_L = 1 / (2\pi RC)$ = Low cut-off frequency of the HPF.

=

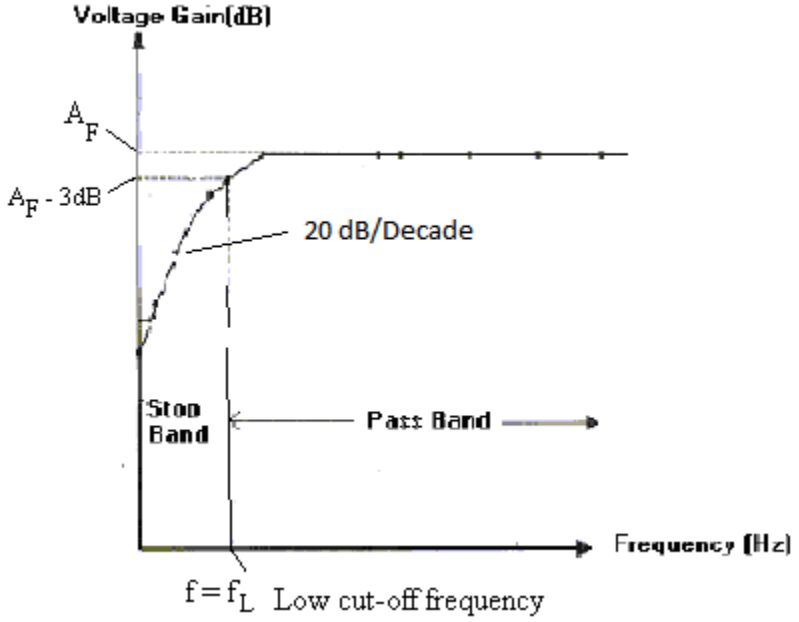
PRACTICAL Cut-off frequency:

f_L = Low cut-off frequency of the HPF.

= 3dB cut-off frequency

=

EXPECTED GRAPH:



RESULT:

QUESTIONS:

1. How filters are classified? Give one example for each classification.
2. What is an active filter and why it is called so?
3. How an active filter differs from a passive filter?
4. What are the advantages of active filters over passive filters?
5. Draw the circuit diagrams of active filters LPF and HPF.
6. Draw the frequency response of all filters (LPF, HPF, BPF, BRF and All-pass).
7. What is the gain roll off rate for a 1st order and 2nd order filter?
8. What is the formula for cut-off frequency?
9. What is a 3 dB frequency and why it is called so?
10. What are the other names for 3 dB frequency?

EXPERIMENT NO: 4 DATE:

IC 741 WAVEFORM GENERATORS – SINE, SQUAREWAVE AND TRIANGULAR WAVES

AIM: To design a Waveform Generator which generates Sine, Square and Triangular waveforms using IC741 and to verify it's various output waveforms.

APPARATUS: Bread Board
CRO
Probes
741 Op-amp, Resistors, Capacitors

THEORY:

Waveform generator using IC741 is a circuit which generates Sine wave, Square wave and Triangular wave. This circuit is a combination of Wien Bridge oscillator, Zero crossing detector (Comparator with zero reference voltage) and Integrator. The Wien Bridge oscillator generates Sine wave which is fed to the input of Zero crossing detector. This detector gives the square wave output which is connected to the input of the Integrator which in turn produces the Triangular wave output.

The frequency of oscillations of the Sine wave output of Wien Bridge oscillator is given by

$$f_o = 1/2\pi RC$$

The frequency of oscillations of Square and Triangular wave outputs will also be the same frequency as that of the Sine wave output.

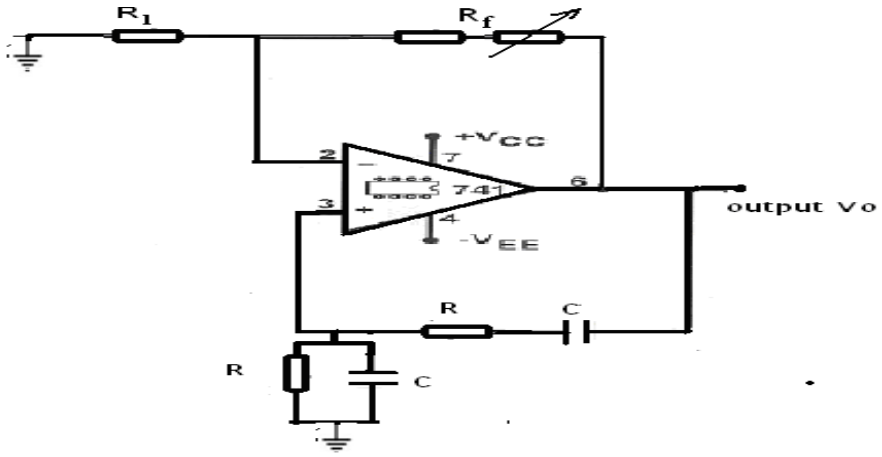
For theory of individual circuits i.e. Wien Bridge oscillator, Zero Crossing Detector and Integrator, please refer to the THEORY section of respective experiments mentioned earlier in this manual.

DESIGN for Wien Bridge Oscillator:

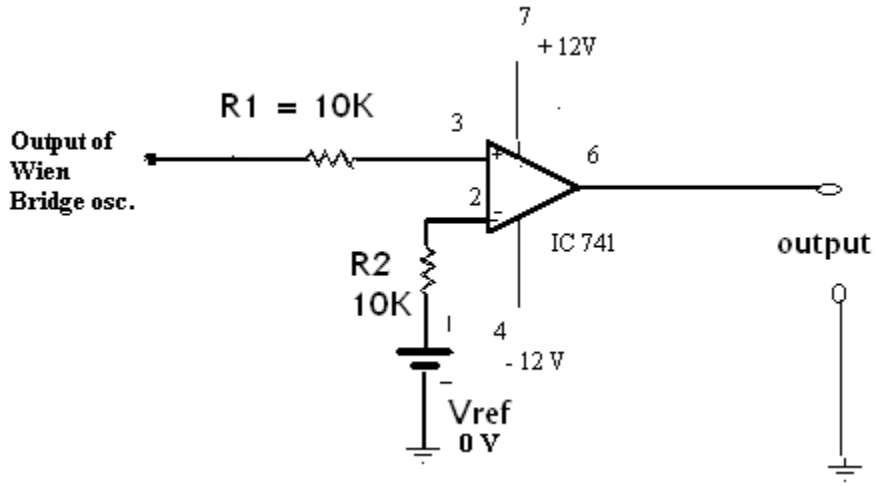
1. Choose a desired frequency of oscillation, say f_o =500 Hz.
2. Choose a value for capacitor C (0.1 μF) and then calculate the value of R by using the equation for f_o ($f_o = 1/2\pi RC$).
3. Choose a value for R_1 (10 KΩ) and calculate the value of R_f from the gain equation ($A_v = 1+R_f/R_1 = 3$). (Note: In practical, the value of R_f may need to be varied to be more than the calculated value.)

CIRCUIT DIAGRAM:

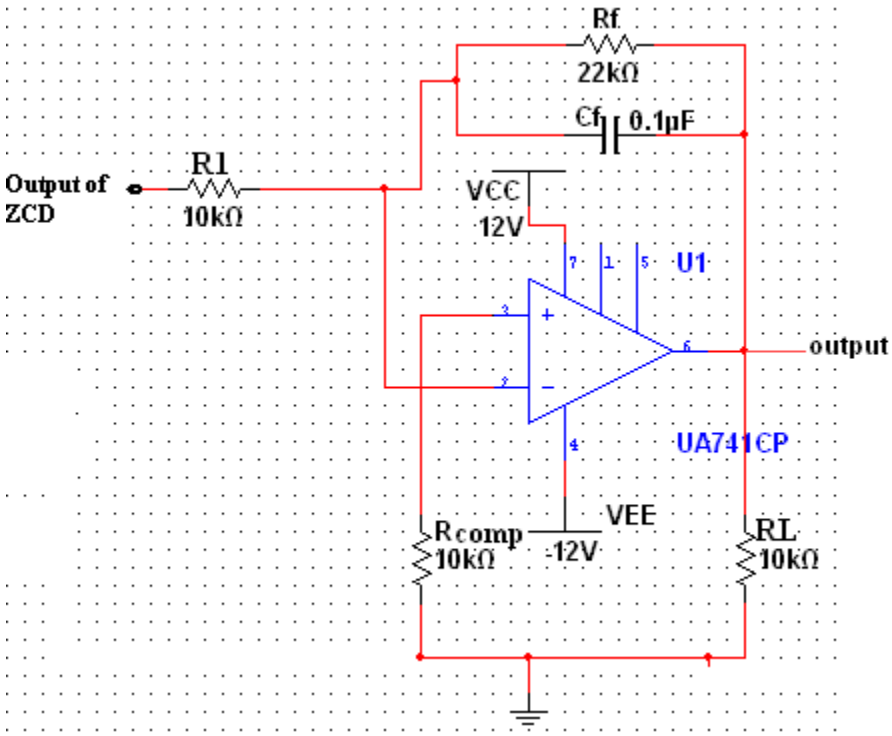
Sine Wave Generator (Wien Bridge Oscillator):



Square Wave Generator (Zero Crossing Detector):



Triangular Wave Generator (Integrator):



PROCEDURE:

Sine wave Generator:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect output to the CRO.
4. Adjust the potentiometer to get an undistorted waveform.
5. Note down the amplitude and the time period, T of the sine wave and calculate the frequency of oscillation, $f_o = 1 / T$.
6. Verify the practical frequency of oscillation calculated in the preceding step with the theoretical value, $f_o = 1/2\pi RC$.
7. Plot the waveform.

Square wave Generator:

1. Switch OFF the power supply.
2. Connect the components/equipment as shown in the circuit diagram.
3. Switch ON the power supply.
4. Connect the input to the channel-1 of CRO and output to the channel-2 of CRO.
5. Observe the square wave output at channel-2 and note down the amplitude and time period, T of the wave form.
6. Verify that the frequency of oscillation of both the input and the output waves is same. Also verify that both the input and the output waves are in same phase.
7. Plot the output waveform in accordance with the input waveform.

Triangular wave Generator:

1. Switch OFF the power supply.
2. Connect the components/equipment as shown in the circuit diagram.
3. Switch ON the power supply.

4. Connect the input to the channel-1 of CRO and output to the channel-2 of CRO.
5. Observe the triangular wave output at channel-2 and note down the amplitude and time period, T of the wave form.
6. Verify that the frequency of oscillation of both the input and the output waves is same. Also verify that the output wave is inverted i.e. 180^o phase shift from the input wave.
7. Plot the output waveform in accordance with the input waveform.

CALCULATIONS:

THEORETICAL Frequency of Oscillation

$f_o = 1/2\pi RC$

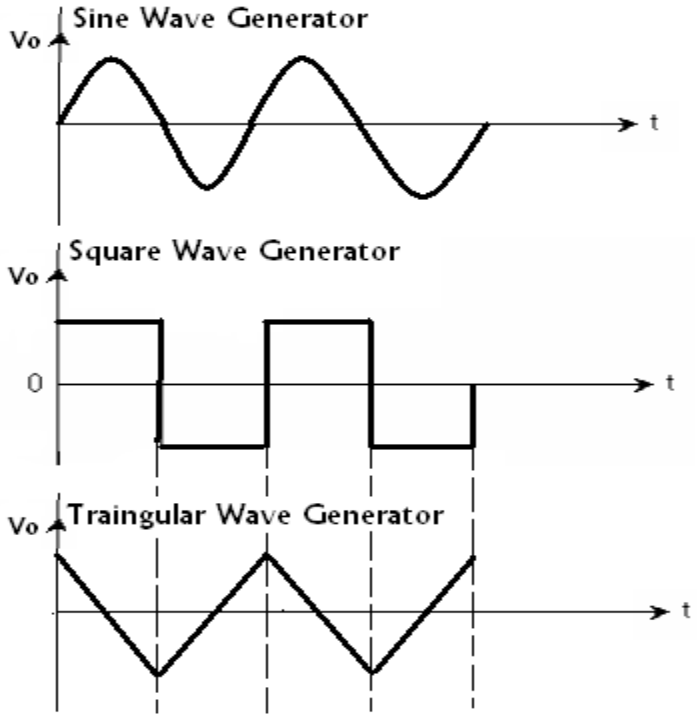
=

PRACTICAL Frequency of Oscillation

$f_o = 1/T$

=

EXPECTED WAVEFORMS:



RESULT:

QUESTIONS:

1. What is a Function Generator?
2. What are the different stages in a Function Generator and how they are connected?
3. Draw the output waveforms at different stages of Function Generator.
4. What is the relationship among the frequencies of output waveforms at different stages of Function Generator?
5. Will there be any phase shift between the input and the output of any stage in the Function Generator and what factor it depends on?
6. Why is R_{comp} used in the circuit of Triangular wave generator?
7. Why is potentiometer used in the circuit of Wien Bridge Oscillator?

EXPERIMENT NO: 5 **DATE**

IC555 TIMER – MONOSTABLE & ASTABLE MULTIVIBRATOR CIRCUITS

a) Monostable Multivibrator

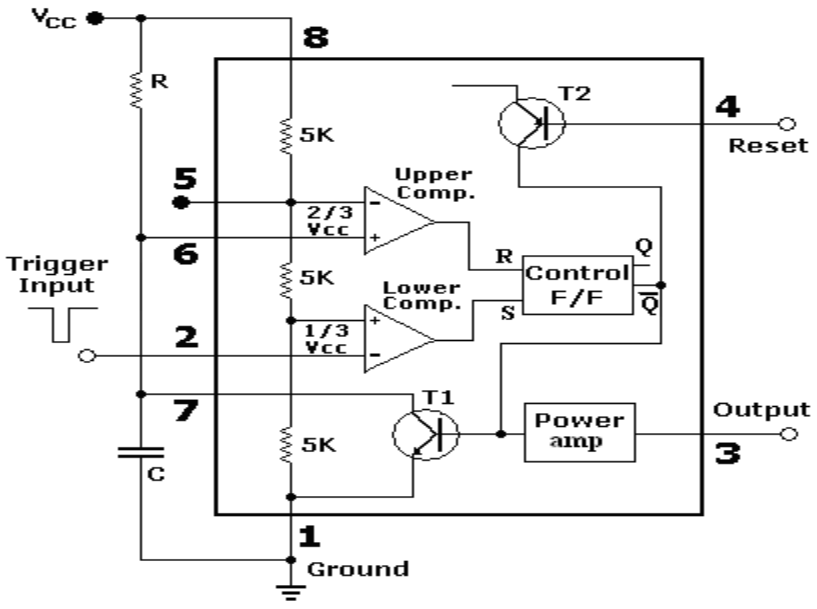
AIM: To design a Monostable Multivibrator using IC555 and compare it's theoretical and practical pulse width.

APPARATUS: Bread Board.
CRO
Probes
Connecting wires
555 Timer, Resistors, Capacitors

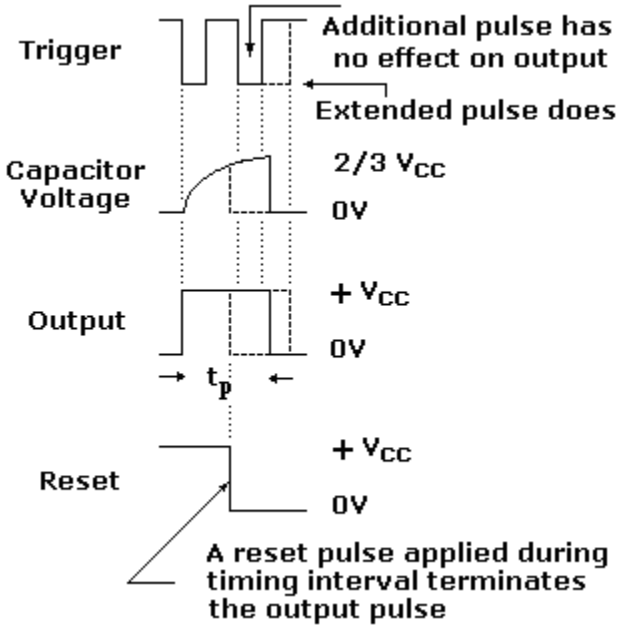
THEORY:

Monostable multivibrator is also called as one–shot Multivibrator. When the output is low, the circuit is in stable state, transistor T1 is ON and Capacitor C is shorted to the ground. However, upon application of a negative trigger pulse to Pin–2, transistor T1 is turned OFF, which releases short circuit across the external capacitor and drives the output High. The capacitor C now starts charging up toward V_{CC} through R. However when the voltage across the external capacitor equals 2/3 $V_{CC,}$ upper comparator's output switches from low to high which in turn derives the output to its low state. And the output of the flip flop turns transistor T1 ON, and hence the capacitor C rapidly discharges through the transistor. The output of the Monostable remains low until a trigger pulse is again applied. Then the cycle repeats. The time during which the output remains high is given by

$$t_p = 1.1\ R\ C$$



Waveforms for IC555 Monostable Multivibrator

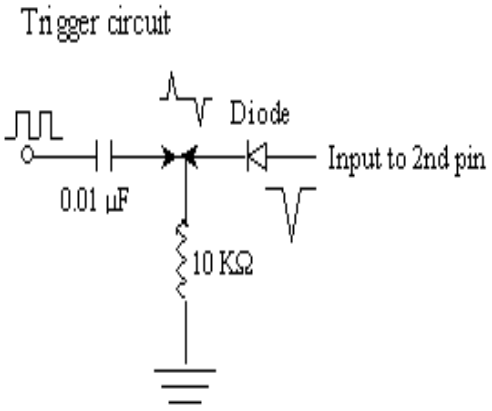


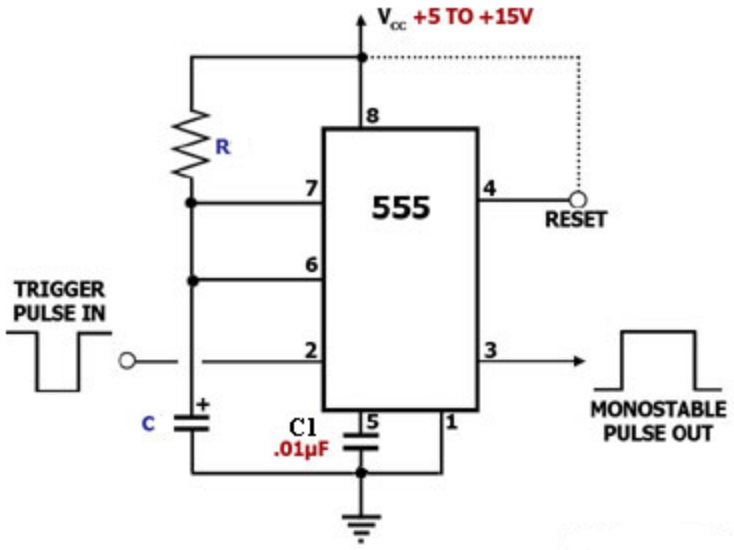
Once triggered, the circuit's output will remain in the high state until the set time t_p elapses. The output will not change its state even if an input trigger is applied again during this time interval t_p.

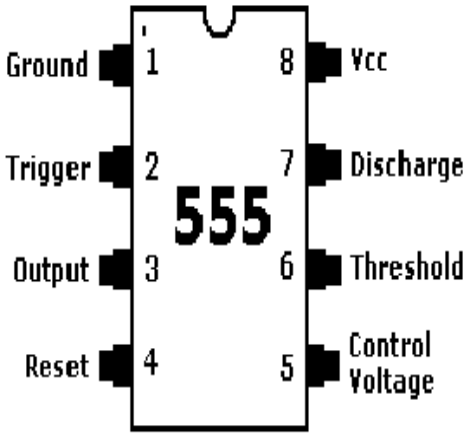
DESIGN:

1. Choose a desired pulse width, say t_p =1.1 ms.
2. Choose a value for capacitor C (0.1 µF) and then calculate the value of R by using the equation for t_p.

CIRCUIT DIAGRAM:







PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect function generator at the trigger input.
4. Connect channel-1 of CRO to the trigger input and channel-2 of CRO to the output (Pin 3).
5. Using Function Generator, apply 1 KHz square wave with amplitude of approx. equal to 9 V_{pp} at the trigger input.
6. Observe the output voltage with respect to input and note down the pulse width and amplitude.
7. Now connect channel-2 of CRO across capacitor and observe the voltage across the capacitor and note it down.
8. Compare the practical pulse width noted in the step above with its theoretical value (t_p=1.1 RC)

CALCULATIONS:

THEORETICAL Pulse width

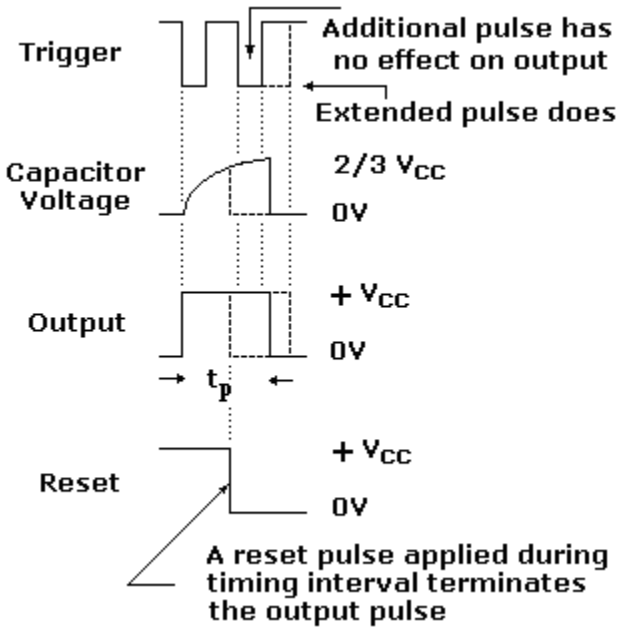
R = C =

t_p = 1.1 RC =

PRACTICAL Pulse width

t_p =

EXPECTED WAVEFORMS:



RESULT:

QUESTIONS:

1. What is the other name for monostable multivibrator (MSMV)?
2. When MSMV is in stable state, what is the output level?
3. Why trigger is required in the case of MSMV?
4. Which type of trigger pulse is required for MSMV?
5. What is the formula for the output pulse width of MSMV?
6. How long MSMV stays in unstable state?

(b) Astable Multivibrator

AIM: To design an Astable Multivibrator using IC555 and compare it's theoretical and practical time period and duty cycle.

APPARATUS: Bread Board.
CRO
Probes
Connecting wires
555 Timer, Resistors, Capacitors

THEORY:

An Astable multivibrator, often called a free-running Multivibrator, is a rectangular-wave-generating circuit. Unlike the Monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determinate by the Two resistors and a capacitor, which are externally connected to the 555 timer.

Figure 1 shows the 555 timer connected as an Astable multivibrator. Initially, when the output is high, capacitor C starts charging towards V_{cc} through R_A and R_B. However as soon as voltage across the capacitor equals 2/3 V_{cc}, comparator 1 triggers the flip-flop, and the output switches low. Now the capacitor C starts discharging through R_B and the transistor Q_1. When the voltage across C equals 1/3 V_{cc}, comparator 2's output triggers the flip-flop, and the output goes high. Then the cycle repeats. The output voltage and the capacitor voltage waveforms are shown in the following figures.

As shown in this figure, the capacitor is periodically charged and discharged between 2/3 V_{cc} and 1/3 V_{cc}, respectively. The time during which the capacitor charges from 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by

$$t_c = 0.69 (R_A + R_B) C \qquad (1)$$

Similarly, the time during which the capacitor discharges from 2/3 V_{cc} to 1/3 V_{cc} is equal to the time the output is low and is given by

$$t_d = 0.69 (R_B)C \qquad (2)$$

Thus the total time period of the waveform is

$$T = t_c + t_d = 0.69(R_A + 2R_B) \qquad (3)$$

Therefore the frequency of oscillation is $f_o = 1/T = 1.45/(R_A + 2R_B)C$

And % Duty cycle $= (t_c/T) *100$ (4)

Circuit Diagram:

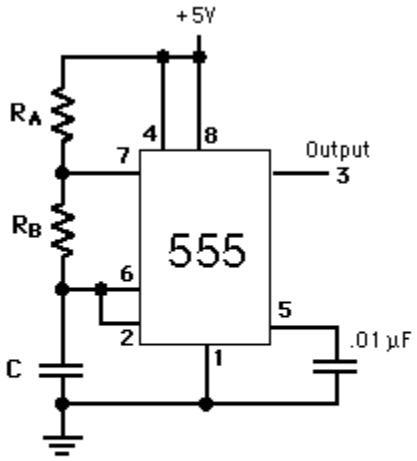
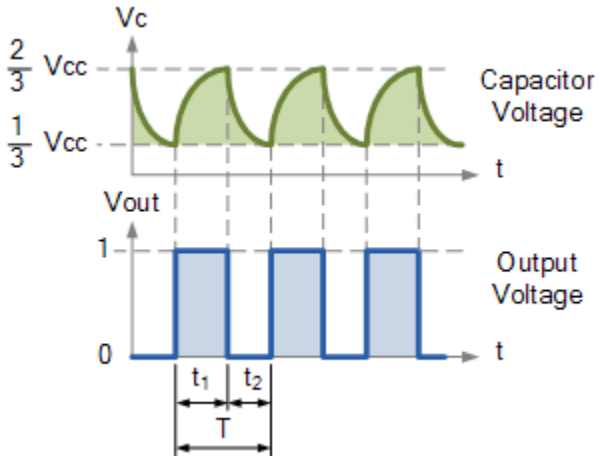


Figure 1: The 555 as an Astable Multivibrator

Expected Wave forms:



PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect channel-1 of CRO to the output (Pin 3).
4. Observe the output voltage and note down the time period and duty cycle.
5. Now connect channel-2 of CRO across capacitor and observe the voltage across the capacitor and note it down.
6. Compare the practical time period and duty cycle.

CALCULATIONS:

THEORETICAL time periods

$t_c = 0.69 (R_A + R_B) C$

$t_d = 0.69 (R_B)C$

Total time period of the waveform, $T = t_c + t_d$

% Duty Cycle = $(t_c / T) *100$

PRACTICAL (from output waveforms)

time period, T =
% Duty cycle =

RESULT:

QUESTIONS:

1. What is the other name for Astable multivibrator (AMV)?
2. What is the formula for the time period of the waveform of AMV?
3. What is the formula for the % of Duty cycle?

EXPERIMENT NO: 6 **DATE**

SCHMITT TRIGGER CIRCUIT USING IC741

AIM: To study the Schmitt trigger characteristics by using IC741 and compare theoretical and practical values of the Upper Threshold voltage, V_{UT} and the Lower Threshold voltage, V_{LT}.

APPARATUS:
741 Op-Amp
Resistors
Bread board
Function generator
CRO
Probes
Connecting wires

THEORY:

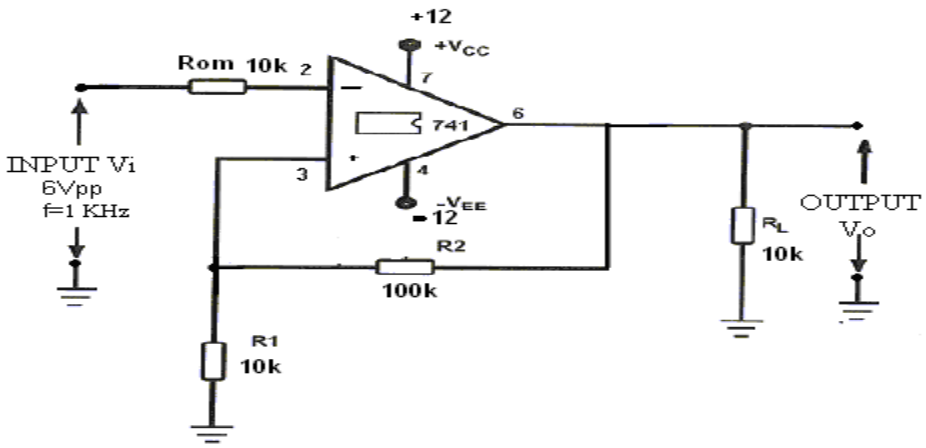
Circuit shows an inverting comparator with positive feedback. This circuit converts an irregular shaped waveform to square wave or pulse. This circuit is known as Schmitt trigger or Regenerative comparator or Squaring circuit. The input voltage V_{in} triggers (changes the state of) the output V_o every time it exceeds certain voltage levels called Upper threshold voltage, V_{UT} and Lower threshold voltage, V_{LT}. The hysteresis width is the difference between these two threshold voltages i.e. $V_{UT} - V_{LT}$. These threshold voltages are calculated as follows.

$V_{UT} = (R_1/R_1+R_2)\ V_{sat}$ when $V_o = V_{sat}$

$V_{LT} = (R_1/R_1+R_2)\ (-V_{sat})$ when $V_o = -V_{sat}$

The output of Schmitt trigger is a square wave when the input is sine wave or triangular wave, where as if the input is a saw tooth wave then the output is a pulse wave.

CIRCUIT DIAGRAM:



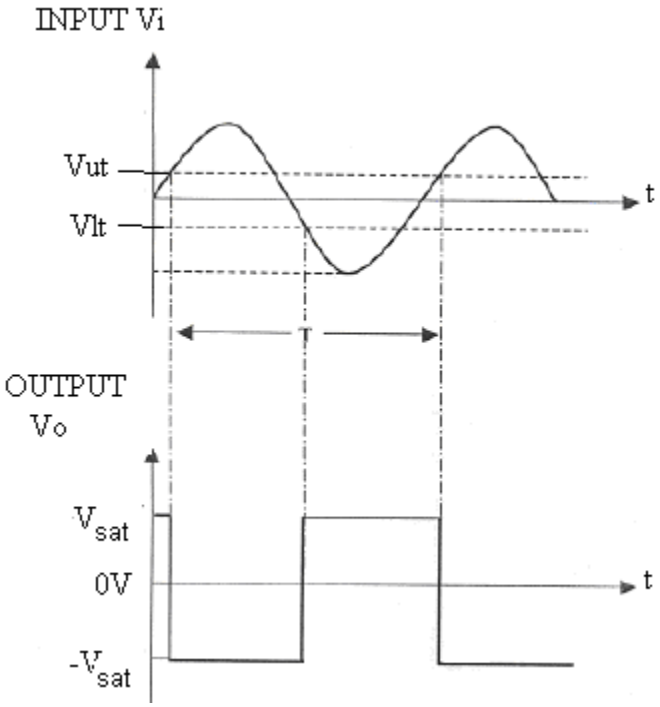
PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.

3. Apply the input sine wave using function generator.
4. Connect the channel–1 of CRO at the input terminals and Channel-2 at the output terminals.
5. Observe the output square waveform corresponding to input sinusoidal signal.

6. Overlap both the input and output waves and note down voltages at positions on sine wave where output changes its state. These voltages denote the Upper threshold voltage and the Lower threshold voltage (see EXPECTED WAVEFORMS below).
7. Verify that these practical threshold voltages are almost same as the theoretical threshold voltages calculated using formulas given in the THEORY section above.
8. Sketch the waveforms by noting down the amplitude and the time period of the input V_{in} and the output V_o.

EXPECTED WAVEFORMS:



Vo versus Vin plot of Hysterisis Voltage

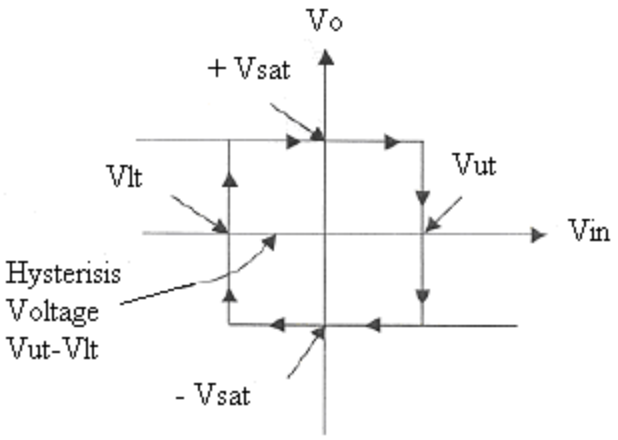


TABLE:

S.No	Theoretical Values				Practical value	
	R_1	R_2	$V_{ut}=\frac{R_1}{R_1+R_2}(+V_{sat})$	$V_{lt}=\frac{R_1}{R_1+R_2}(-V_{sat})$	V_{ut}	V_{lt}
1						
2						
3						

RESULT:

QUESTIONS:

1. Which is type of comparator called Schmitt trigger using IC741?
2. What is the output wave of Schmitt trigger if the input is sine wave?
3. What type of waveform is obtained when triangular or ramp waveforms are applied to Schmitt trigger circuit?
4. Explain how a square wave is obtained at the output of timer when sine wave input is given?
5. What is the Threshold voltage?
6. How do you calculate the theoretical values of V_{UT} and V_{LT} in the case of IC741?
7. What is the Hysteresis width?
8. What is the minimum amplitude of the input sine wave in the case of Schmitt trigger using IC741?

EXPERIMENT NO: 7 **DATE**

IC565 – PLL APPLICATION

AIM:

1. To study the operation of NE565 PLL
2. To use NE565 as a multiplier

EQUIPMENTSANDCOMPONENTS:

APPARATUS

1. DC power supply	-	1 No.
2. CRO	-	1 No.
3. Breadboards	-	1 No.
4. Function Generator	-	1 No.

THEORY

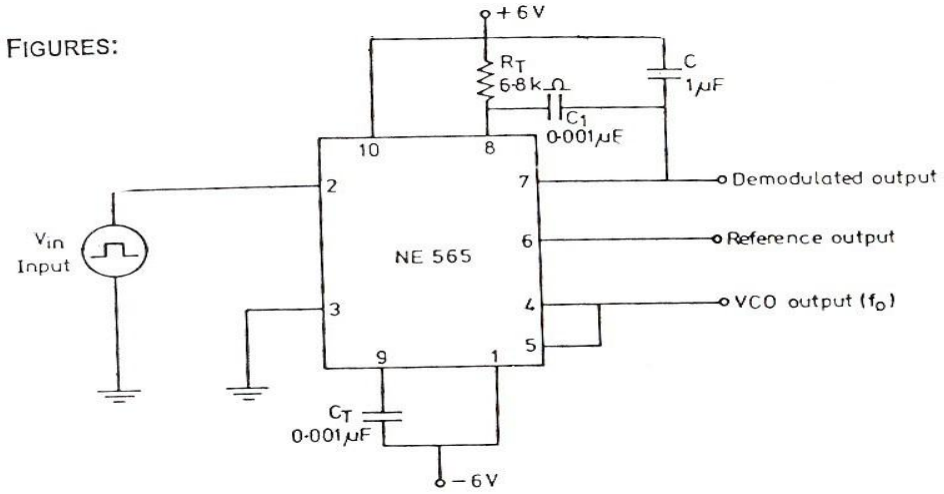
The 565 is available as a14-pin DIP package. It is produced by Signatic Corporation. The output frequency of the VCO can be rewritten as

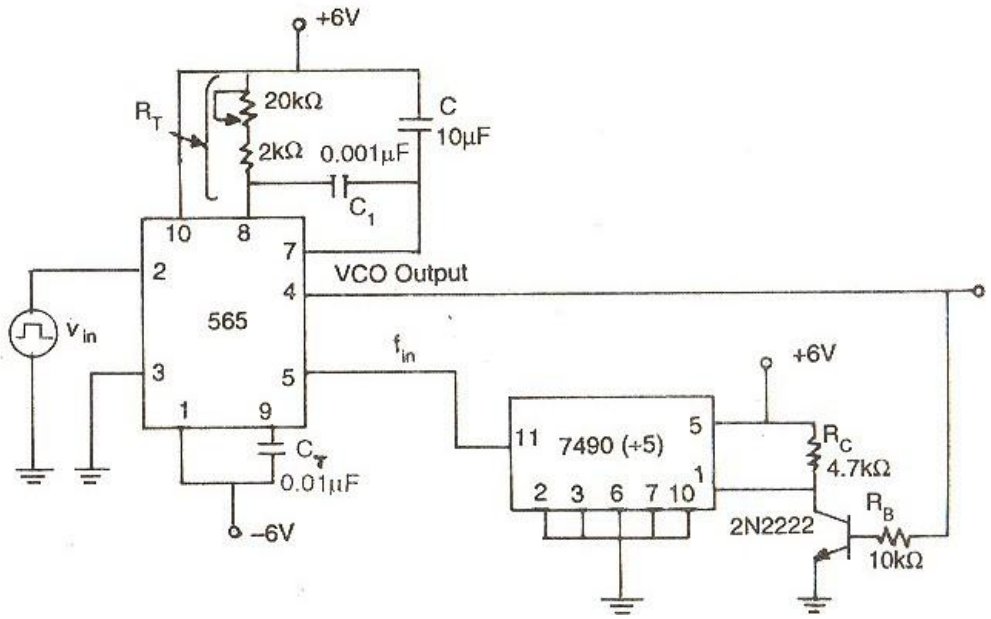
$$f_o = 0.25 / R_T C_T \text{ Hz.}$$

Where R_T and $C_T$are the external resistor and capacitor connected to pin8 and pin9. A value between 2k and 20k is recommended for R_T .The VCO free running frequency is adjusted with R_T and C_T to be at the centre for the input frequency range.

CIRCUIT DIAGRAM

FIGURES:





PROCEDURE:

i. Connect the circuit using the component values as shown in the figure
ii .Measure the free running frequency of VCO at pin4 with the input signal V_{in}set= zero. Compare it with the calculated value=$0.25/R_TC_T$
iii. Now apply the input signal of 1Vpp square wave at a1kHz to pin2
iv. Connect1st channel of the scope to pin2 and display this signal on the scope.
v .Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower ends of the capture range. Go on increase the input frequency; till PLL tracks the input signal, say to a frequency f_2.This frequency f_2 gives the upper end of the lock range. If the input frequency is increased further the loop will get unlocked.

vi. Now gradually decrease the input frequency till the PLL is a gain locked. This is the frequency f_3, the upper end of the capture range .Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range
vii. The lock range $f_L=(f_2-f_4)$ compare it with the calculated value of $(7.8\ f_o/12)$
Also the capture range is $f_c=(f_3-f_1)$. Compare it with the calculated value of capture range.

$$f_c = [f_L / (2)(3.6)(10^3)C]^{1/2}$$

viii To use PLL as a multiplier,make connections as show in fig. The circuit uses a 4-bit binary counter7490 used as a divide-by-5circuit.
ix. Set the input signal at 1Vpp square wave at 500Hz
x..Vary the VCO frequency by adjusting the 20K potentiometer till the PLL is locked. Measure the output frequency.
xi. Repeat step9 and10 for input frequency of 1kHz and 1.5kHz.

OBSERVATIONS:

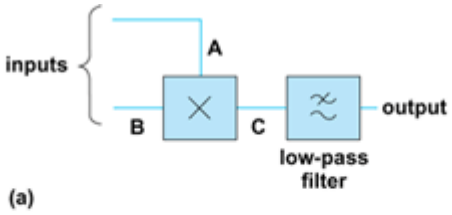
f_O =
f_L =
f_C =

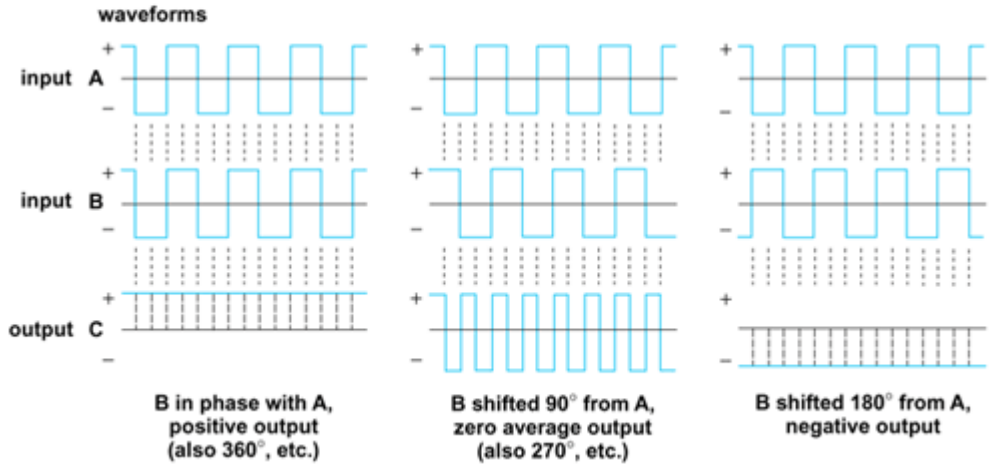
CALCULATIONS:

$f_L = (f_2 - f_4) = 7.8f_O /12$

$f_C = (f_3 - f_1) = [f_L/(2)\ (3.6)(10^3)C]^{1/2}$

GRAPH:





RESULT:

f_O =

f_L =

f_C =

EXPERIMENT No: 8 **DATE**

VOLTAGE REGULATOR USING IC 723, THREE TERMINAL VOLTAGE REGULATORS – 7805, 7809, 7912

AIM

To study the Fixed Voltage Regulators (1) 7805
(2) 7809
(3) 7812
(4) 7912
(5) 723 Variable Voltage Regulator

Theory

DC power for electronic circuits is most conveniently obtained from commercial ac lines by using rectifier - filter system, called a dc power supply. The rectifier-filter combination constitutes an ordinary dc power supply . The dc voltage from an ordinary power supply remains constant so long as ac mains voltage or load is unaltered . However, in many electronic applications, it is desired that dc voltage should remain constant irrespective of changes in ac mains or load. Under such situations, voltage regulating devices are used with ordinary power supply. This constitutes regulated dc power supply and keeps the dc voltage at fairly constant value.

ORDINARY DC POWER SUPPLY

An ordinary or regulated dc power supply contains a rectifier and a filter circuit as shown in Fig-1. The output from the rectifier is pulsating dc. These pulsations are due to the presence of ac component in the rectifier output. The filter circuit removes the ac component so that steady dc voltage is obtained across the load.

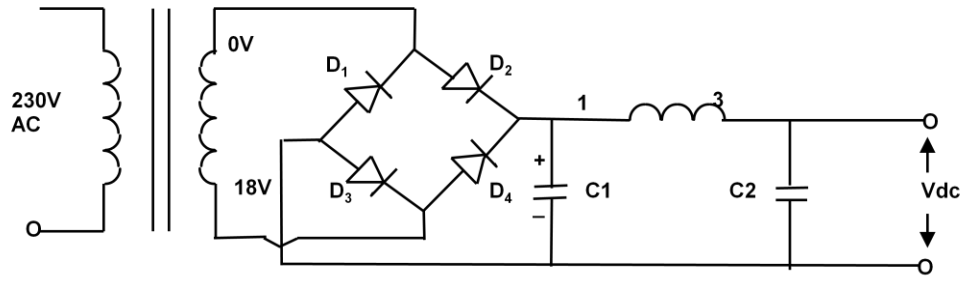


Fig -1.

Limitations : An ordinary dc power supply has two following drawbacks:

1. The dc output voltage changes directly with input ac voltage.
2. The dc output voltage decreases as the load current increases. This is due to voltage drop in (a) Transformer windings (b) Rectifier (c) Filter circuit

These variations in dc output voltage may cause inaccurate or erratic operation or even malfunctioning of many electronic circuits. Eg. In an oscillator, the frequency will shift and in transmitters, distorted output will result, Therefore, ordinary power supply is unsuited for many applications and is being replaced by regulated power supply.

For comparison of different types of power supplies, the following terms are commonly used:

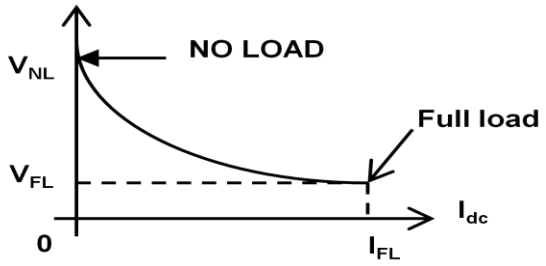
1. Voltage regulation : The dc voltage available across the output terminals of a given power supply depends upon load current. If the load current Idc is increased by decreasing RL as in Fig-

2, there is greater voltage drop in the power supply and hence smaller dc output voltage will be available . Reverse will happen if the load current decreases. The variation of output voltage w.r.t. the amount of load current drawn from
the power supply is known as voltage regulation and is expressed by the following relation:

% voltage regulation = $(V_{NL} - V_{FL}) / V_{FL} * 100$

V_{NL} = dc output voltage at no load.

V_{FL} = dc output voltage at full load



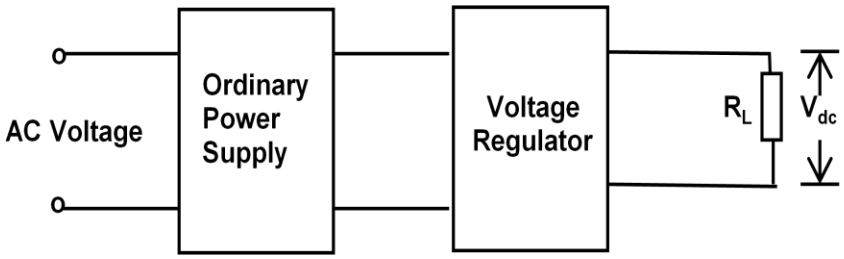
In a well designed power supply, the full load voltage is only slightly less than no -load voltage I.e. voltage regulation approaches zero. Therefore, lower the voltage regulation, the lesser the difference between full-load and no-load voltage and better is the power supply. Power supplies used in practice have a voltage regulation of 1% i.e. full load voltage is within 1% of the no-load voltage. Fig-3 shows the change of dc output voltage with load current. This is known as voltage regulation curve.

2. MINIMUM LOAD RESISTANCE : The change of load connected to a power supply varies the load current and hence the dc output voltage. In order that a power supply gives the rated output voltage and current, there is minimum load resistance allowed. For instance, I a power supply is required to deliver a full-load current I_{FL} at full load voltage V_{FL}, then,

$$R_{L\ (min)} = \frac{V_{FL}}{I_{FL}}$$

REGULATED POWER SUPPLY

A dc power supply which maintains the output voltage constant irrespective of ac mains fluctuations or load variations is known as regulated dc power supply. A regulated power supply consists of an ordinary power supply and voltage regulating device an in fig-4. The output of ordinary power supply is fed to the voltage regulator which produces the final output. The output voltage (Vdc) remains constant whether the load current changes or there are fluctuations in the input ac voltage.



NEED : In an ordinary power supply, the voltage regulation is poor i.e dc output voltage changes appreciably with load current. Moreover, output voltage also changes due to variations in the input ac voltage. This is due to the following reasons:-

i) In practice, there are considerable variations in ac line voltage caused by outside factors beyond our control. This changes the dc output voltage. Most of the electronic circuits will refuse to work satisfactorily on such output voltage fluctuations. This necessitates to use regulated dc power supply.
ii) The internal resistance of power supply is relatively large (>30W). Therefore, output voltage is markedly affected by the amount of load current drawn from the supply. These variations in dc voltage may cause erratic operation of electronic circuits. Therefore, regulated dc power supply is the only solution in such situations.

HARDWARE SPECIFICATIONS

1. Built - in 16V - 0 - 16V / 350mA
   12V - 0 - 12V / 350mA
   8V - 0 - 8V / 350mA AC sources
2. Bridge rectifier using IN4007 diodes - 1No.
3. Filter capacitors (470μF / 35V) - 2Nos.
4. Fixed Voltage Regulator 7805 - 1No.
   7809 - 1No.
   7812 - 1No.

   7912 - 1No.
5. Variable Voltage Regulator using 723 IC

EXPERIMENTAL PROCEDURE

1. Connect the circuit as shown in fig - 4.

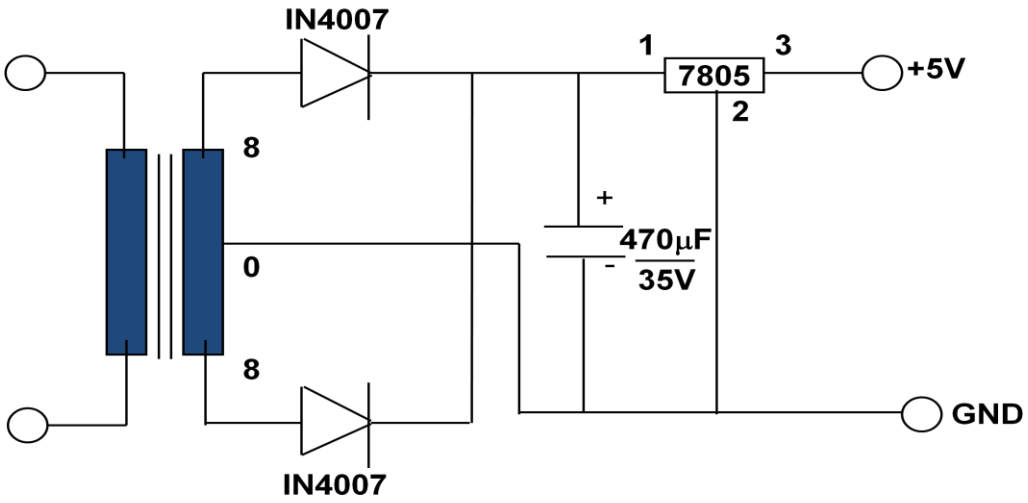


Fig - 4

2. Connect different load resistors available in the front panel, note down the output current and voltage.
3. Also test the circuit with 12V - 0 - 12V, 16V - 0 - 16V AC sources also.
4. Remove 7805 and connect 7809, 7812 also repeat 2 and 3 steps.
5. Connect the circuit shown in fig - 5.

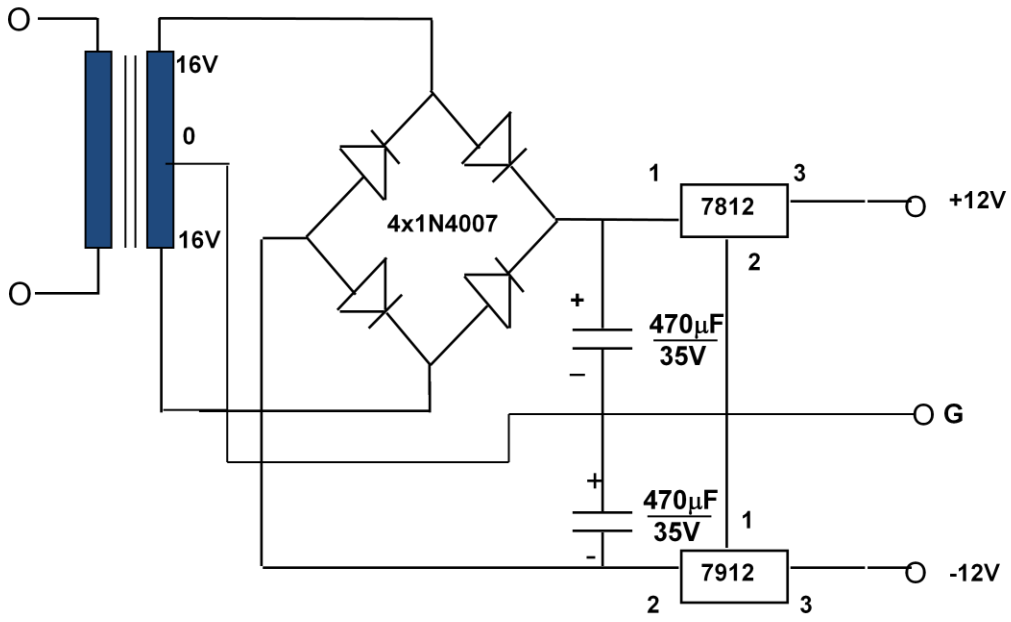


Fig - 5

723 Regulator

It is a monolithic voltage regulator constructed on a single silicon chip. The device consists of a temperature compensated reference amplifier,, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass element may be used when output currents exceeding 150mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above the device features low stand by current drain, low temperature drift and high ripple rejections. The 723 is intended for use with positive or negative supplies as a series, shunt , switching or floating regulator. Applications include laboratory power supplies, air borne systems and other power supplies for digital and linear circuits.

CIRCUIT DESCRIPTION

Fig -4 shows the circuit of a variable regulator constructed with 723 IC. Pin is connected to positive terminal of the supply. 10KW potentiometer connected to pin 4, controls the output voltage. Output is available at Pin10. This output is not sufficient to drive loads. So it is passed through the Darlington pair of transistors (CL100).

EXPERIMENTAL PROCEDURE

1. Switch ON the experimental board by connecting power card to the AC mains.
2. Make sure that the potentiometer are in minimum position.
3. Connect the 8V AC tapping of the transformer secondary to the bridge rectifier input and short Raw DC +Ve point and pin 12 of 723 (See Fig-)
4. Measure the output voltage with a DMM and also measure the output with the 10KW potentiometer with its maximum position.
5. Now, disconnect the 8V AC tapping and connect 10V AC tapping and notedown the minimum and maximum output voltages with 10KW minimum and maximum positions.
6. Repeat the same procedure for 12V, 16V and 18V AC transformer secondary tapings and tabulate these values in Table-1.
7. Now, again connect 8V AC to the bridge rectifier input, set the output DC voltage at 5V with 10KW potentiometer.
8. Connect the load resistor with (0-50mA) milliammeter and vary the load resistor and note down the readings of the output voltage and output current with different load resistor.

9. Tabulate these values in Table-2.

S.No.	AC INPUT (RMS Volts)	DC OUTPUT minimum	maximum
1.	8V	2.96V	5.58V
2.	10V	3.00V	5.69V
3.	12V	3.03V	5.77V
4.	16V	3.08V	5.89V
5.	18V	3.10V	5.90V

Table -1

S.No.	LOAD CURRENT I_{OUT} (mA)	OUTPUT VOLTAGE V_{OUT} (volts)
1.	49mA	5.27V
2.	45mA	5.30V
3.	40mA	5.32V
4.	35mA	5.36V
5.	30mA	5.40V
6.	25mA	5.41V
7.	20mA	5.43V
8.	15mA	5.50V
9.	10mA	5.5V
10.	5mA	5.5V

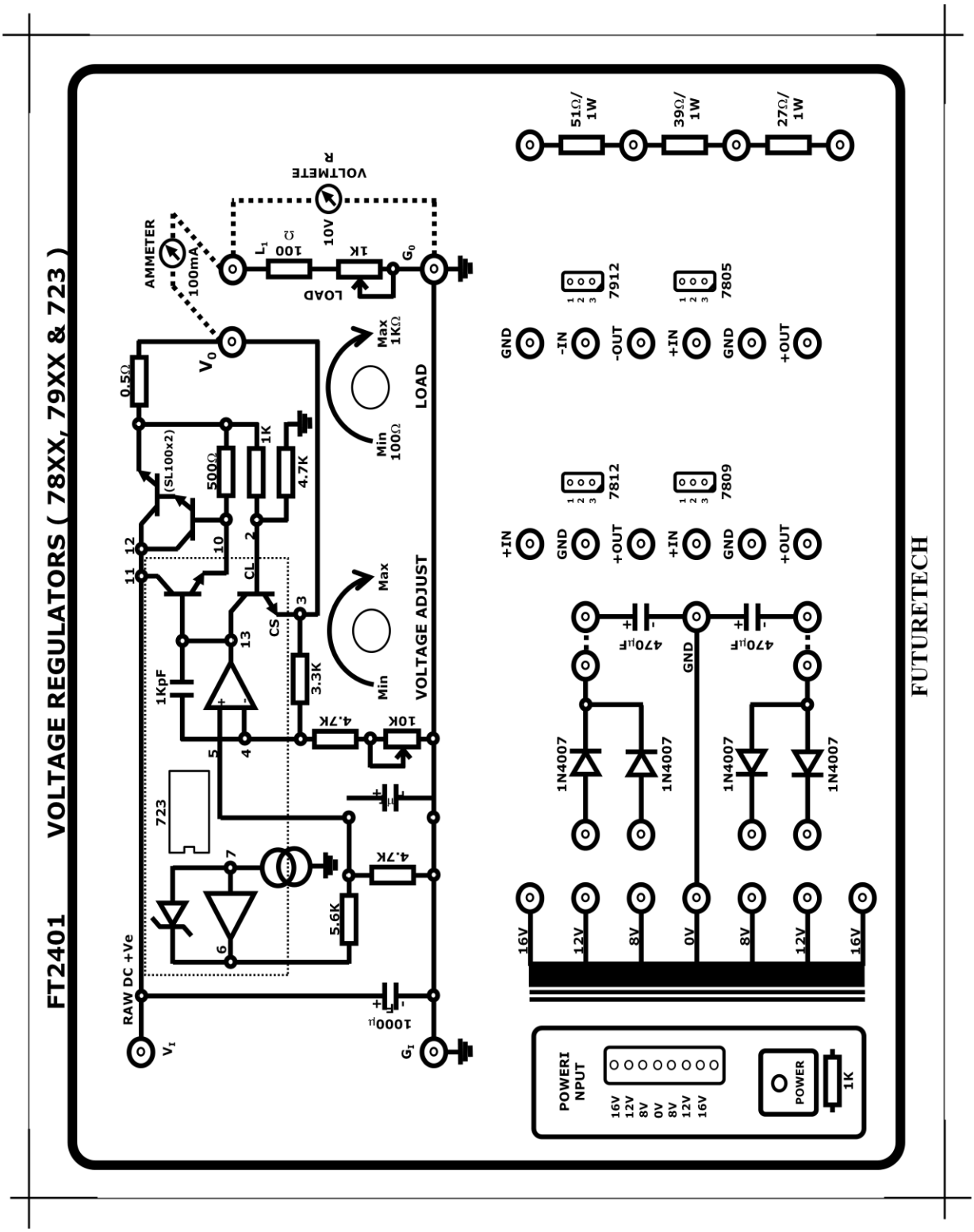
Table -2

LOAD REGULATION

10. Calculate & Tabulate the load regulation at each load current.

% Regulation $= (V_{NL} - V_{FL})/V_{FL} * 100$

11. Draw a graph between load current I_{dc} & load voltage V_{dc} regulation.


FT2401 VOLTAGE REGULATORS (78XX, 79XX & 723)
FUTURETECH
VOLTMETER
AMMETER
100mA
LOAD
10V
1K
100Ω
0.5Ω
500Ω
1K
4.7K
(SL100x2)
Max 1KΩ
Min 100Ω
LOAD
VOLTAGE ADJUST
Max
Min
3.3K
1KpF
4.7K
10K
5.6K
723
1000µF
RAW DC +Ve
51Ω/ 1W
39Ω/ 1W
27Ω/ 1W
7912
7805
7812
7809
GND
-IN
-OUT
+IN
+OUT
470µF
1N4007
16V
12V
8V
0V
POWER INPUT
POWER
1K

RESULT:

CYCLE - II

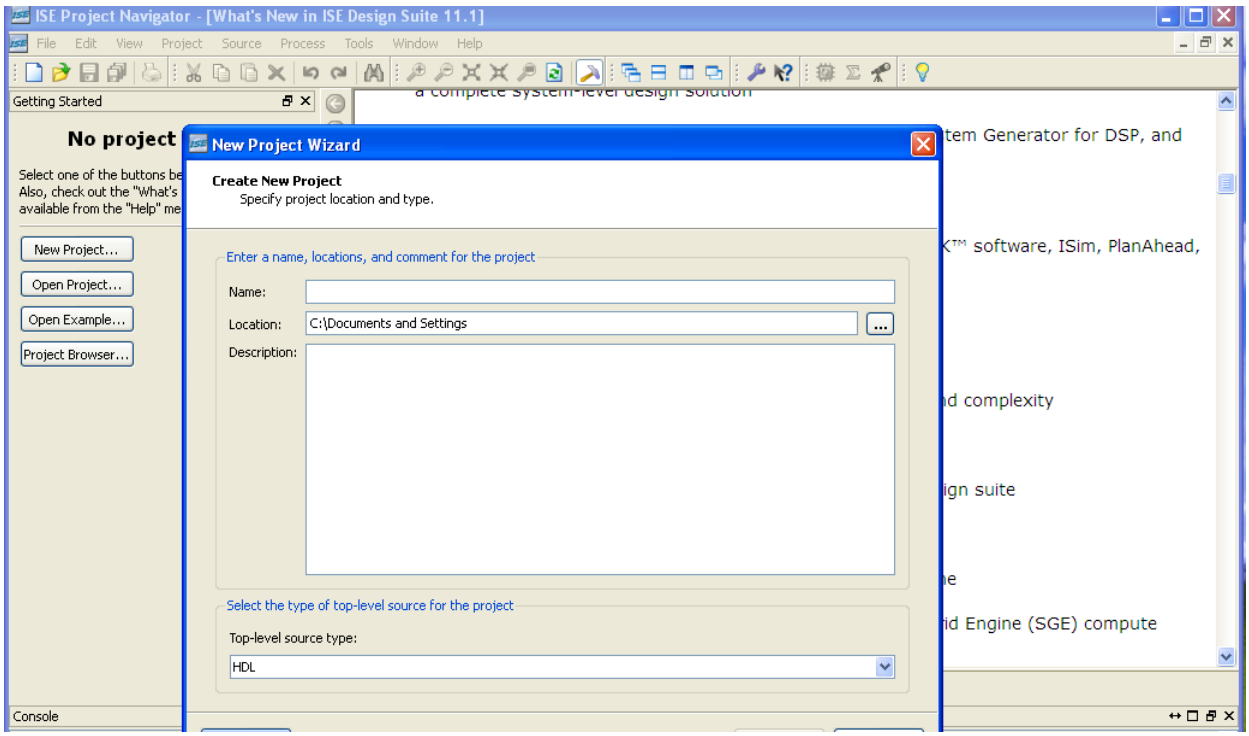
INTRODUCTION - XILINX

Xilinx ISE is a software tool produced by Xilinx for synthesis and analysis of HDL designs, which enables the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

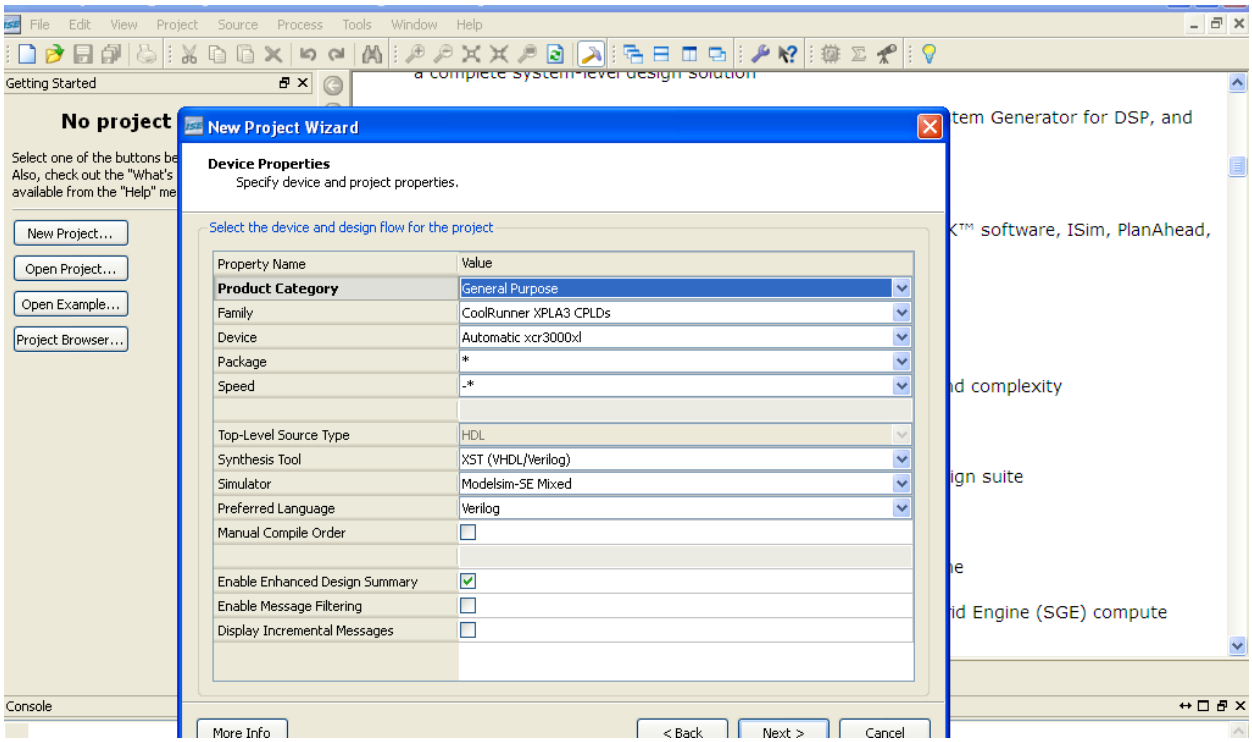
In our Lab, the scope is limited to design and analyze the design using test benches & simulation.
The following is the step by step procedure to design in the Xilinx ISE:

1. ***New Project Creation***

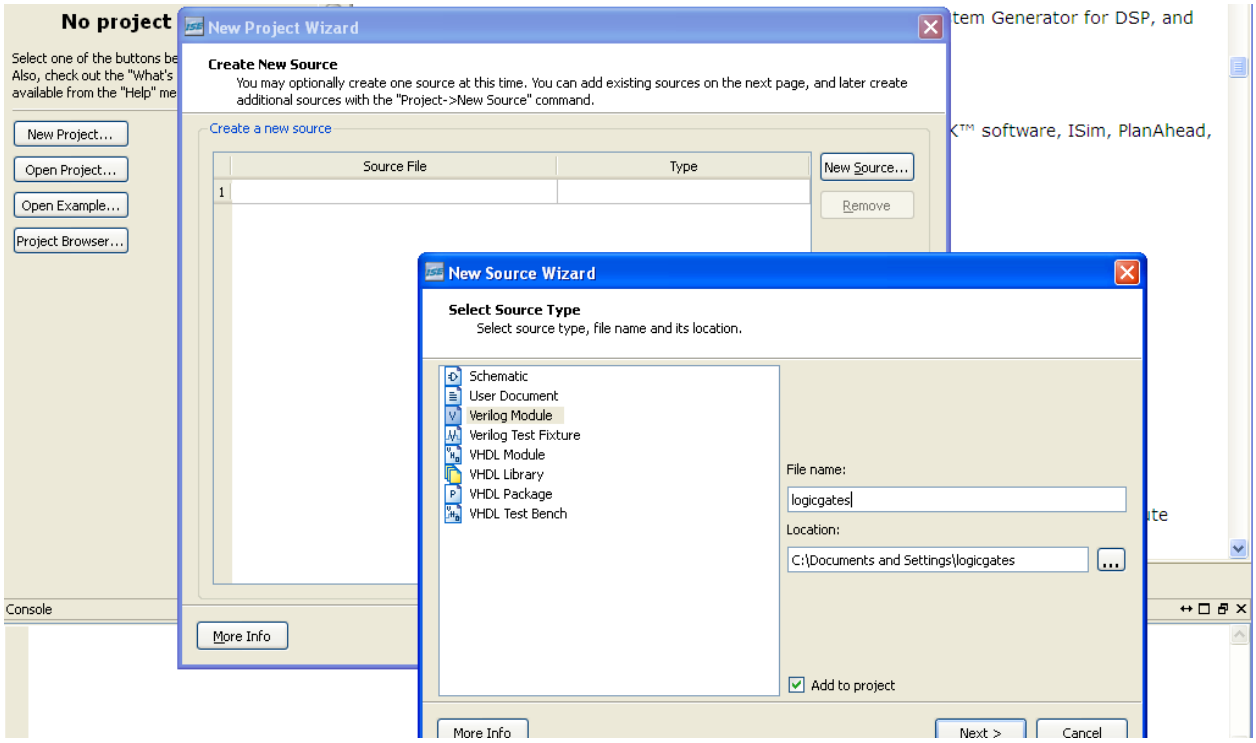
   Once the Xilinx ISE Design suite is started, open a new project & enter your design name and the location path. By default 'HDL' is selected as the top-level source type. (If not, please select Top-level source type as 'HDL')



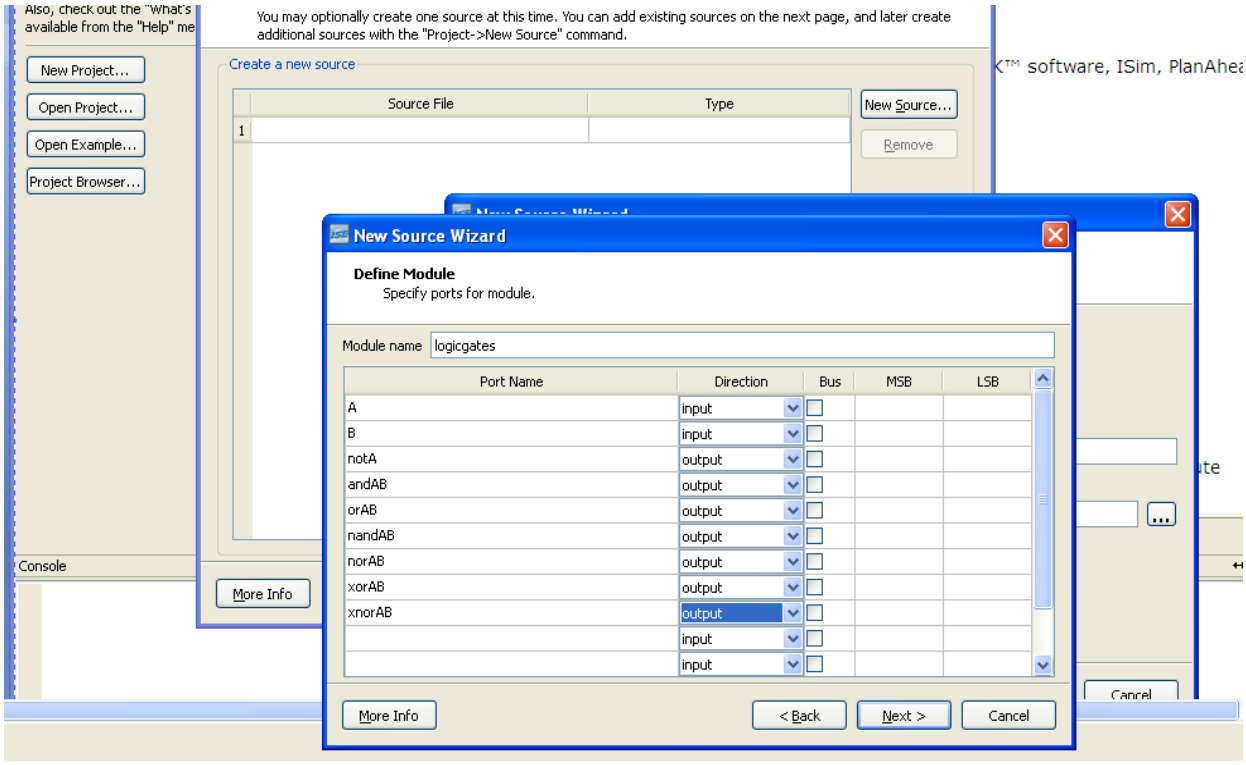
2. Continue to the next window and check if the Preferred Language is selected as 'Verilog'



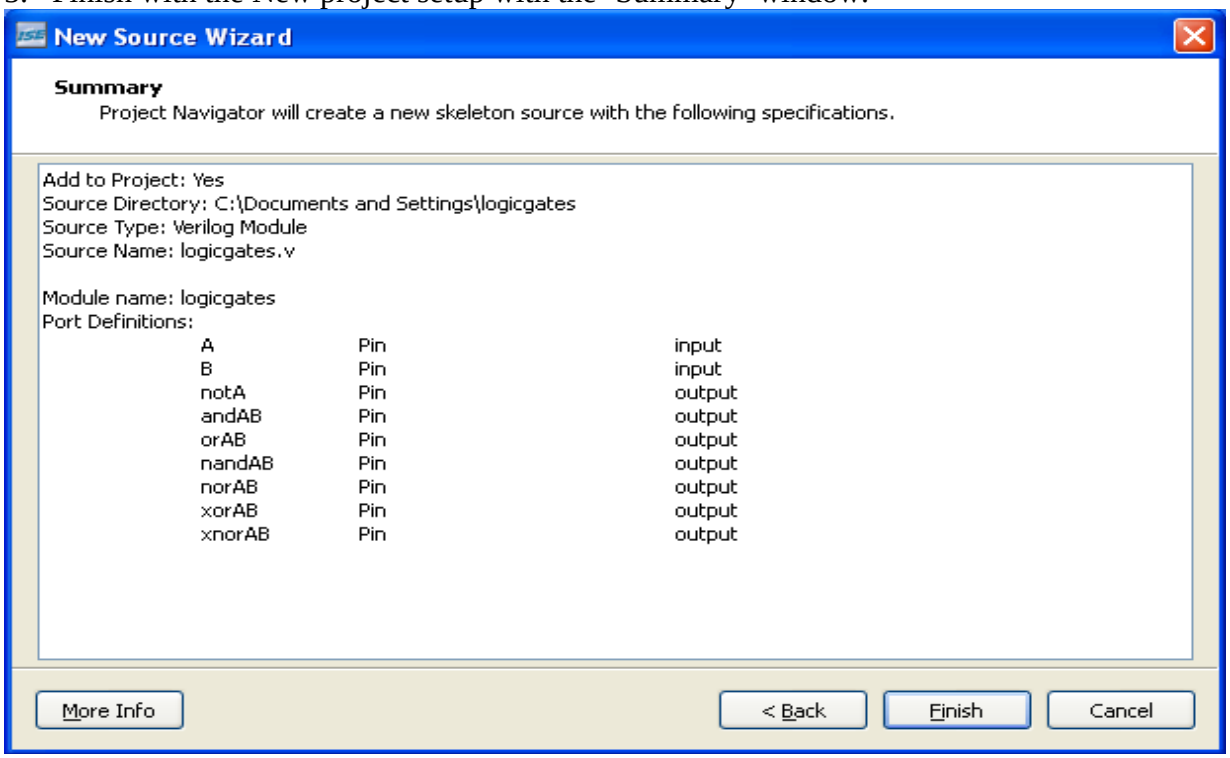
3. Proceed by clicking 'Next' and create a 'New Source' using the 'Create New Source' Window



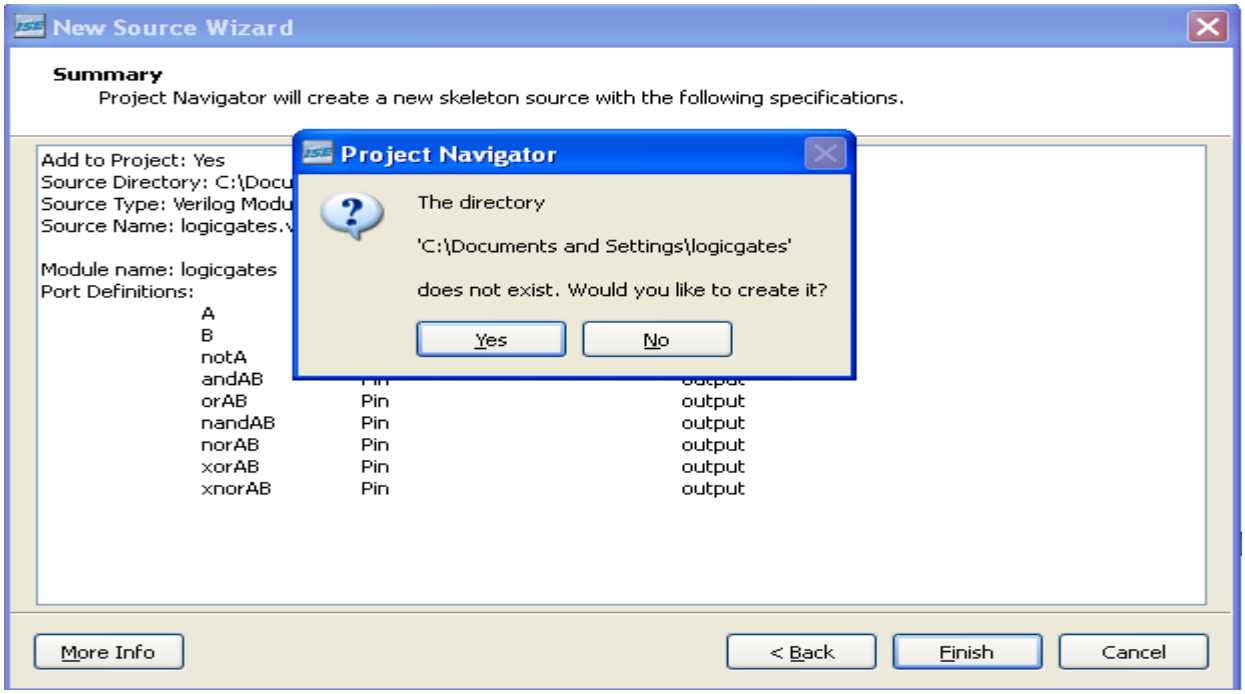
4. Select the source type as ‘Verilog Module’ and input a filename and proceed to ‘Next’. In the next window ‘Define Module’ enter the ports.



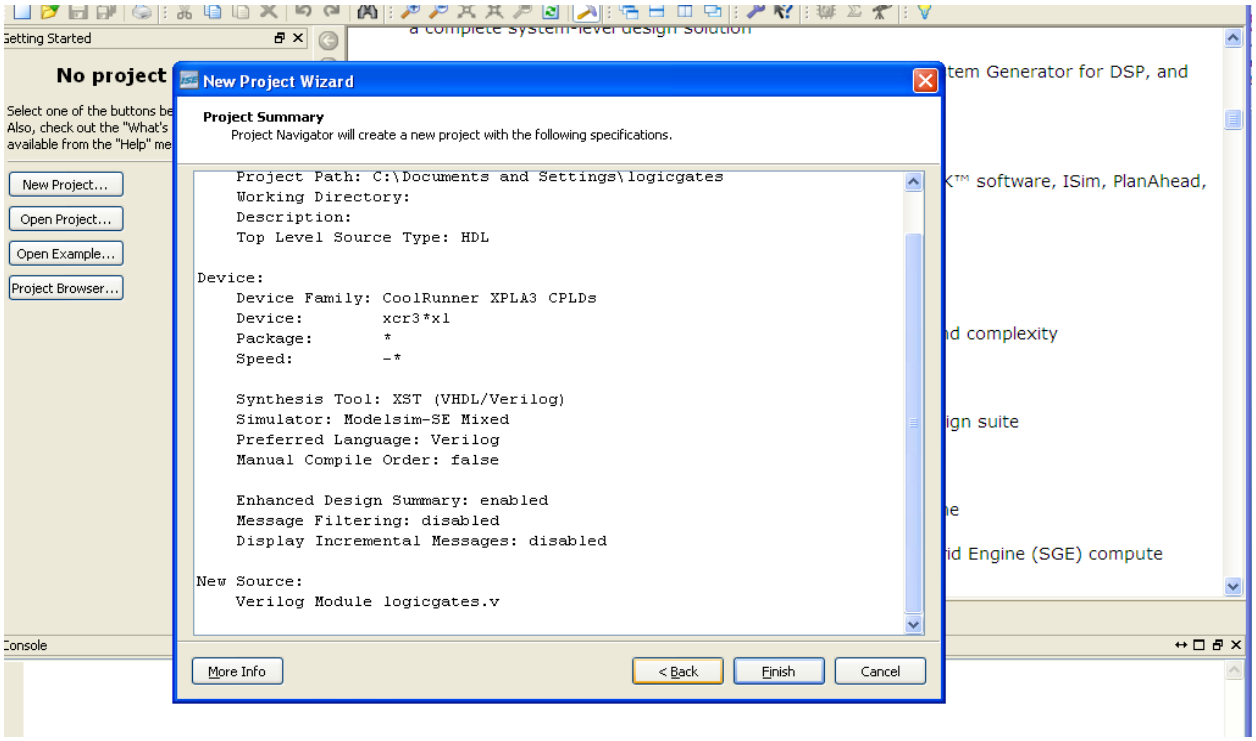
5. Finish with the New project setup with the ‘Summary’ window.



6. Once ‘Finish’ is selected a pop-up appears to create the directory. Select ‘yes’

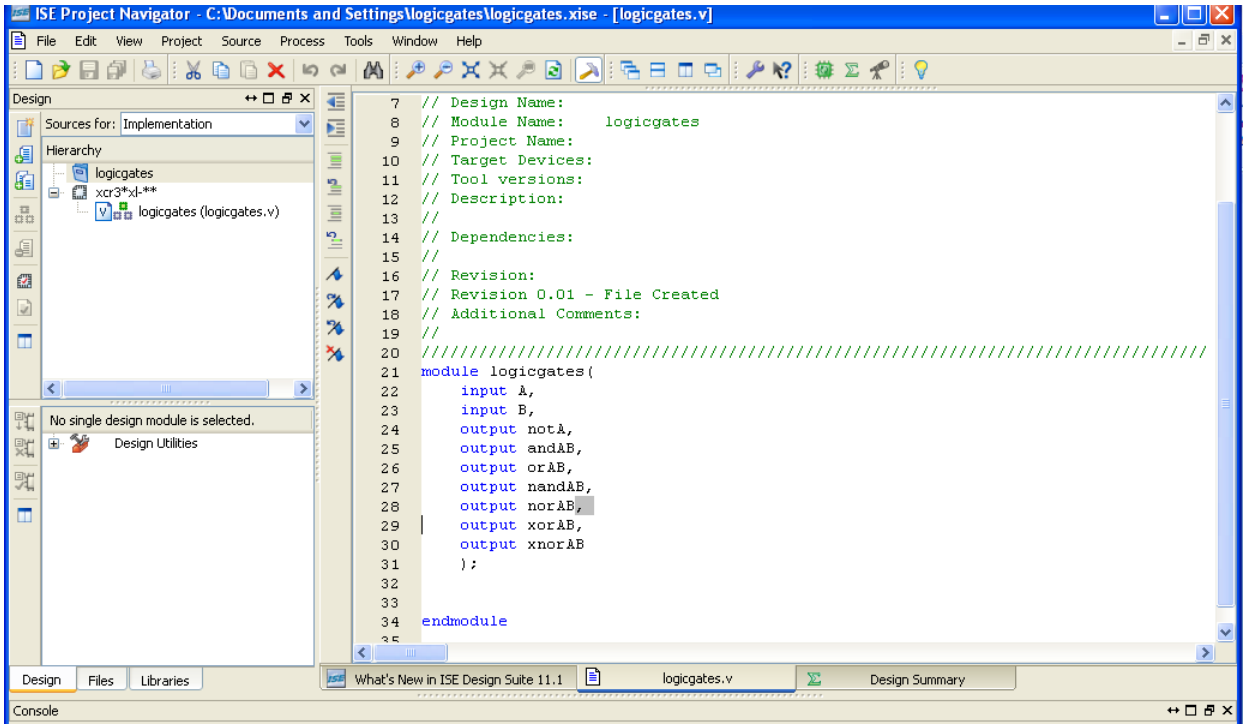


7. Then proceed to ‘Next’ in the “New Project Wizard’ to ‘Add Existing Sources’. ‘Add source’ if an existing source is available, If not proceed to ‘Next’ and finish with the ‘Project Summary’ window

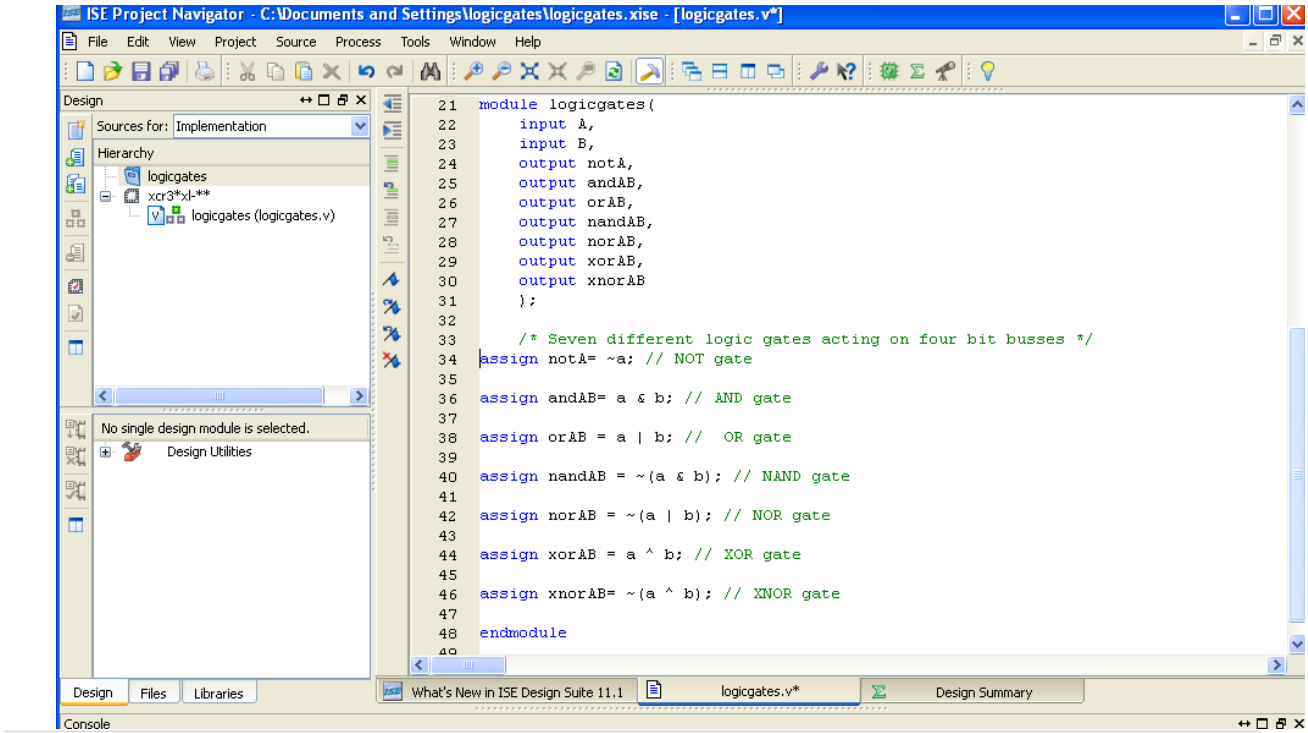


8. Design Entry and Syntax Check

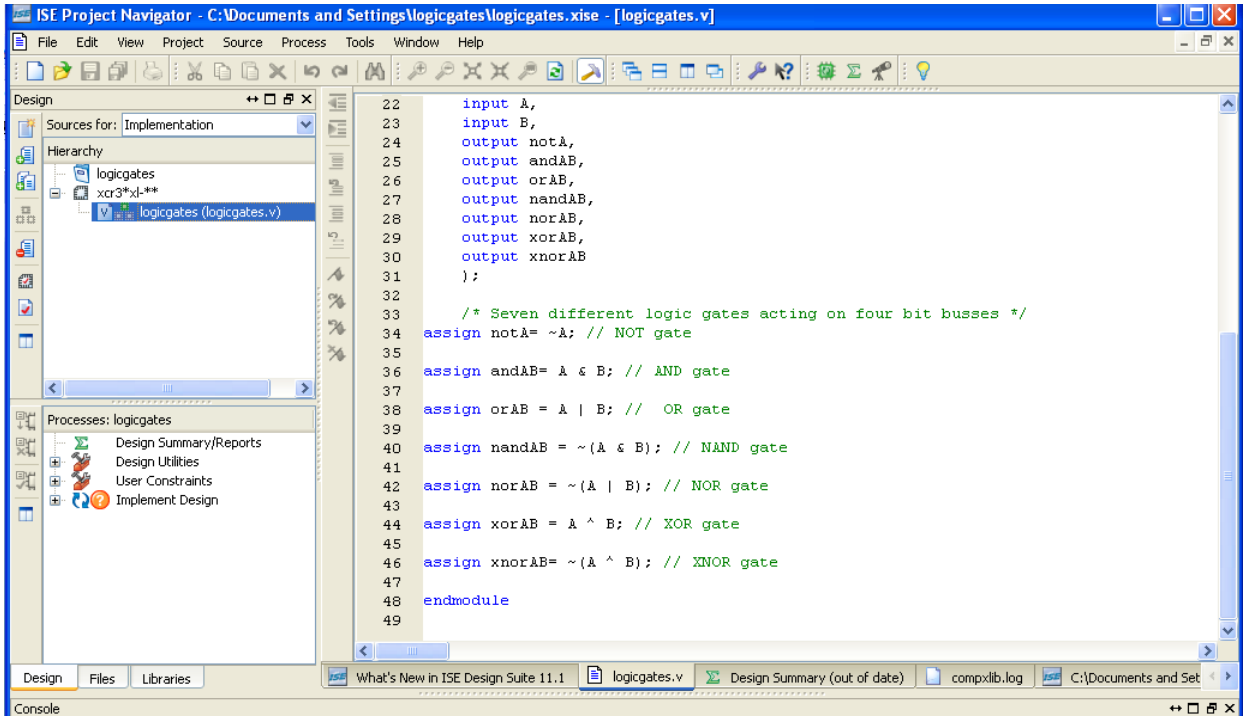
The ports defined during the 'Project Creation' are defined as a module in the 'filename.v' file



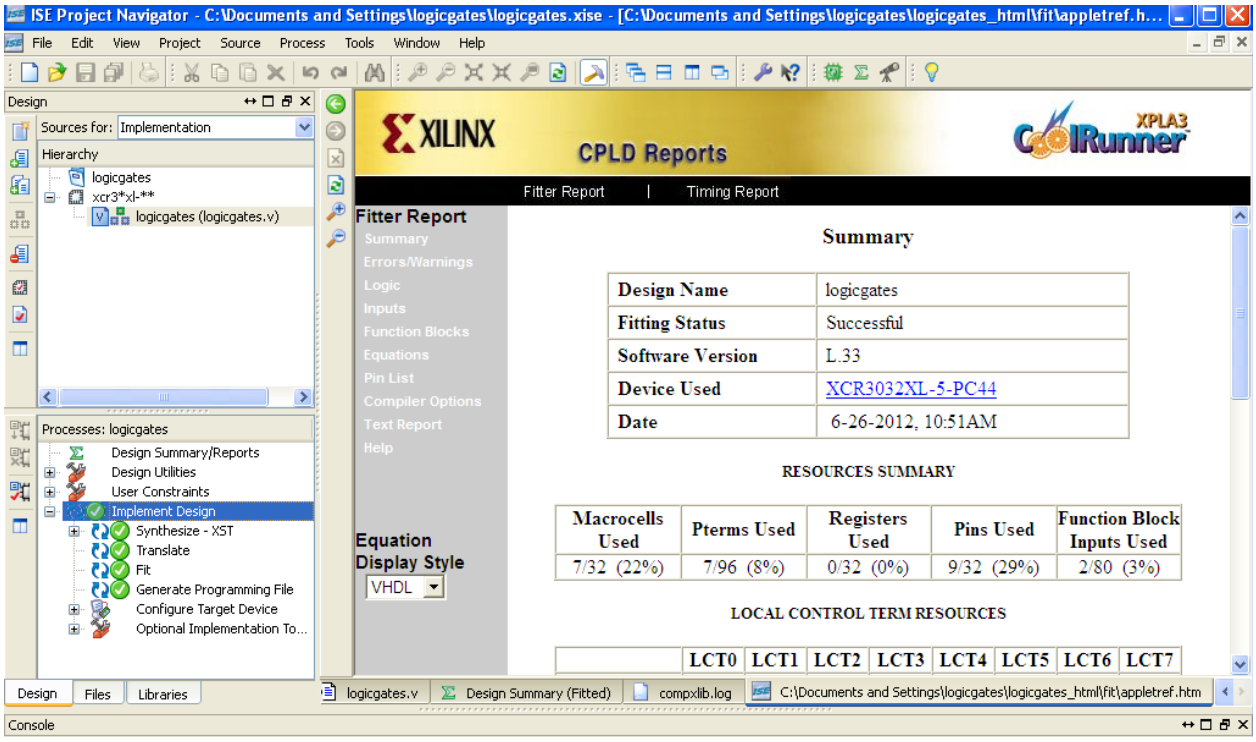
9. Input your design (verilog code) within the module definition



10. Select the design from the 'Hierarchy'window. In the below window of Processes 'Implement Design 'would be orange (in color) ready for implementation

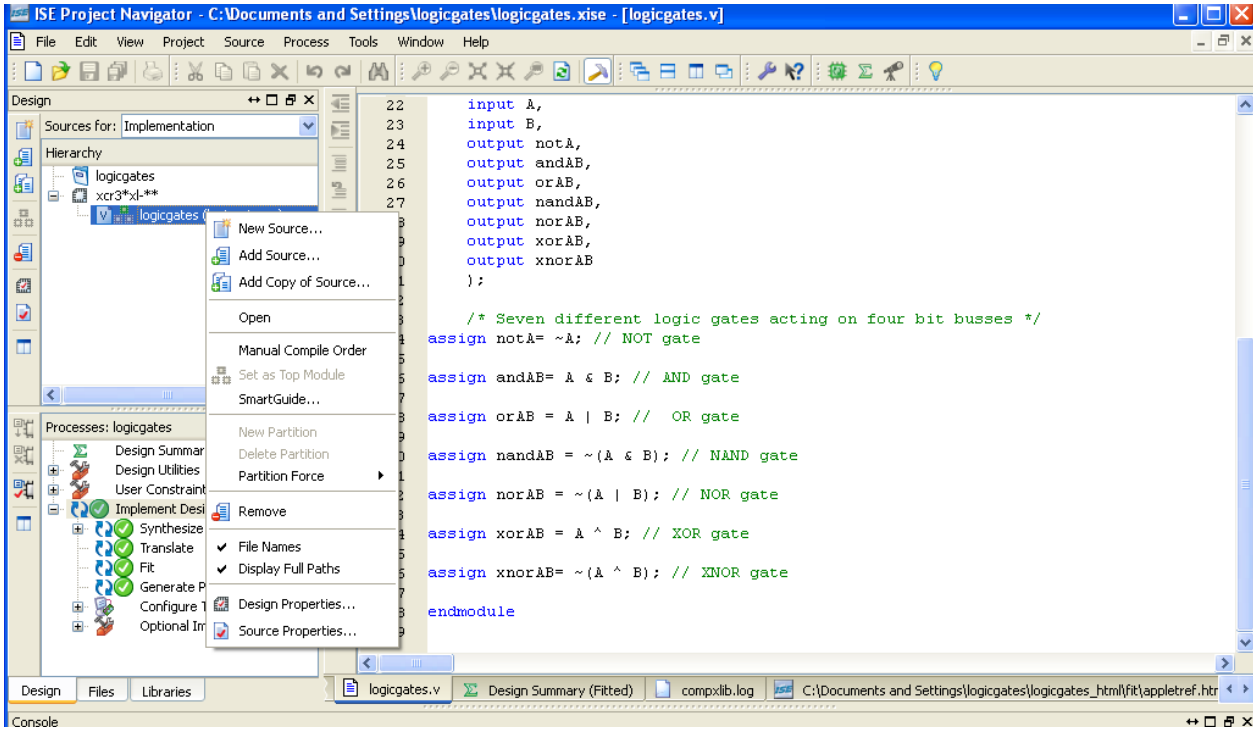


11. Double click on implement design, it turns green (in color) once the design is implemented successfully and the Summary report is displayed.

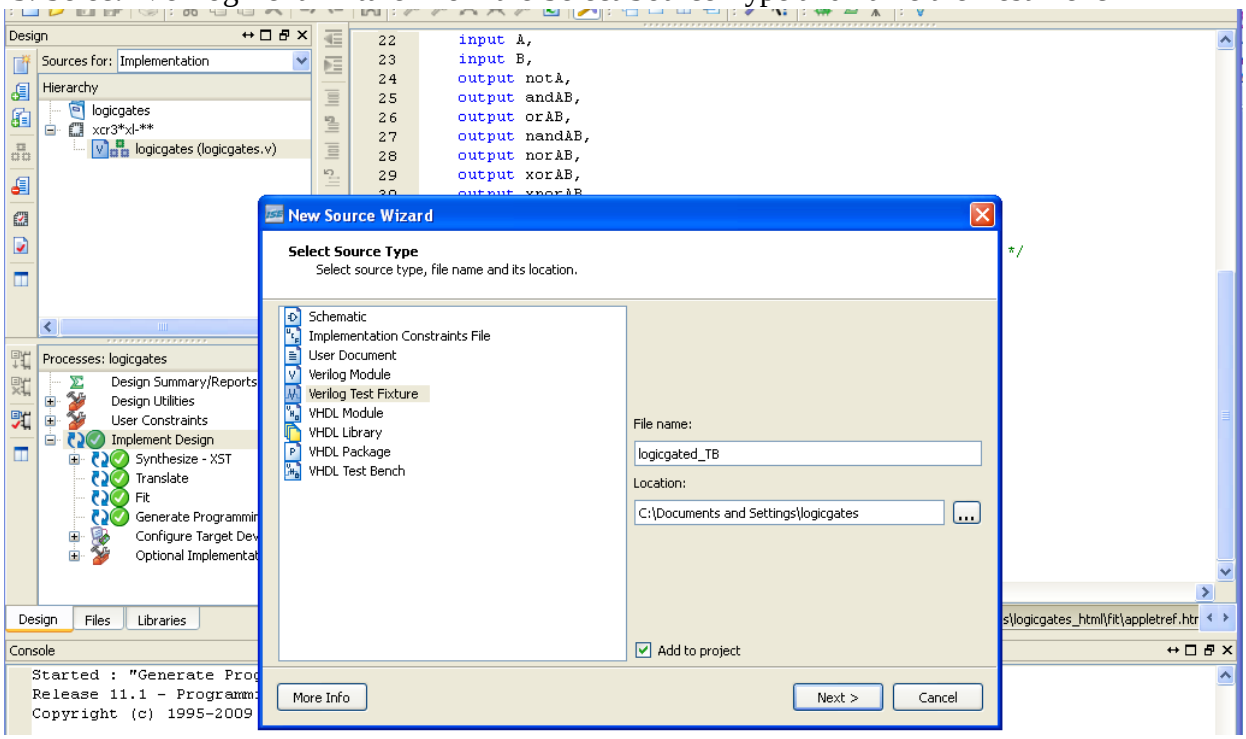


12. Test-Bench creation, Simulation & Verification

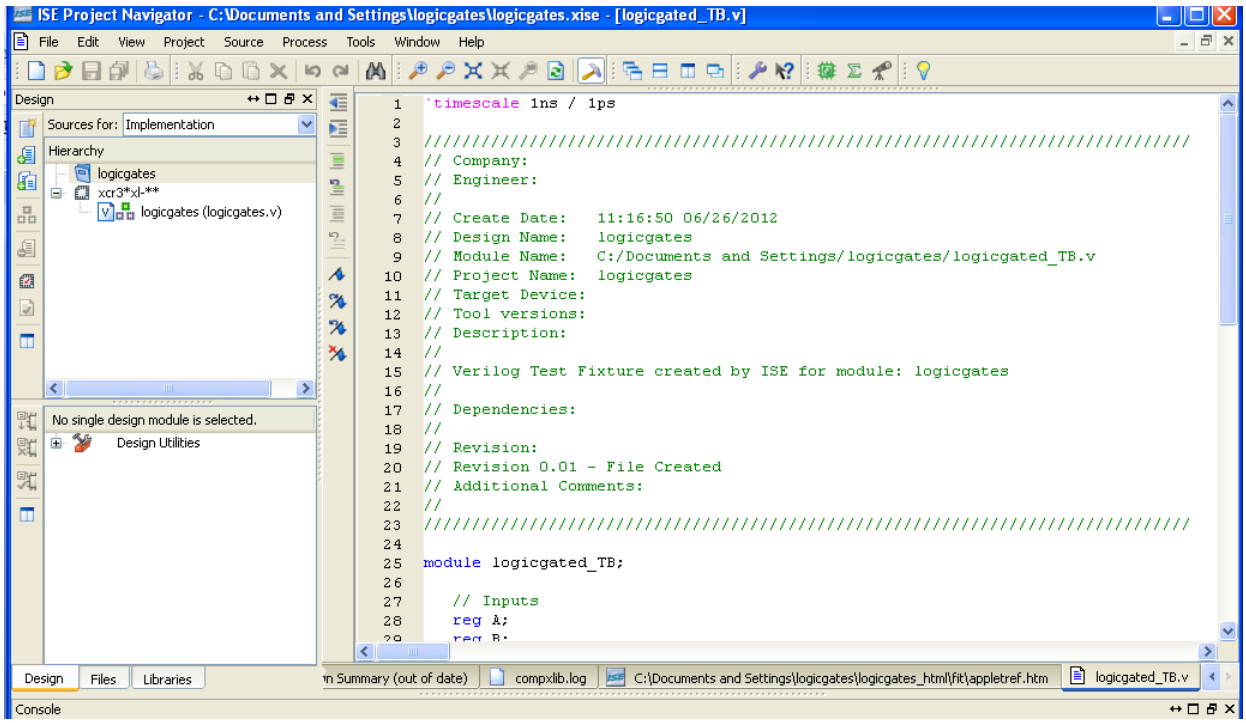
To add a test-bench to the existing design, right click on the '.v' file from the Hierarchy window and select 'New Source'



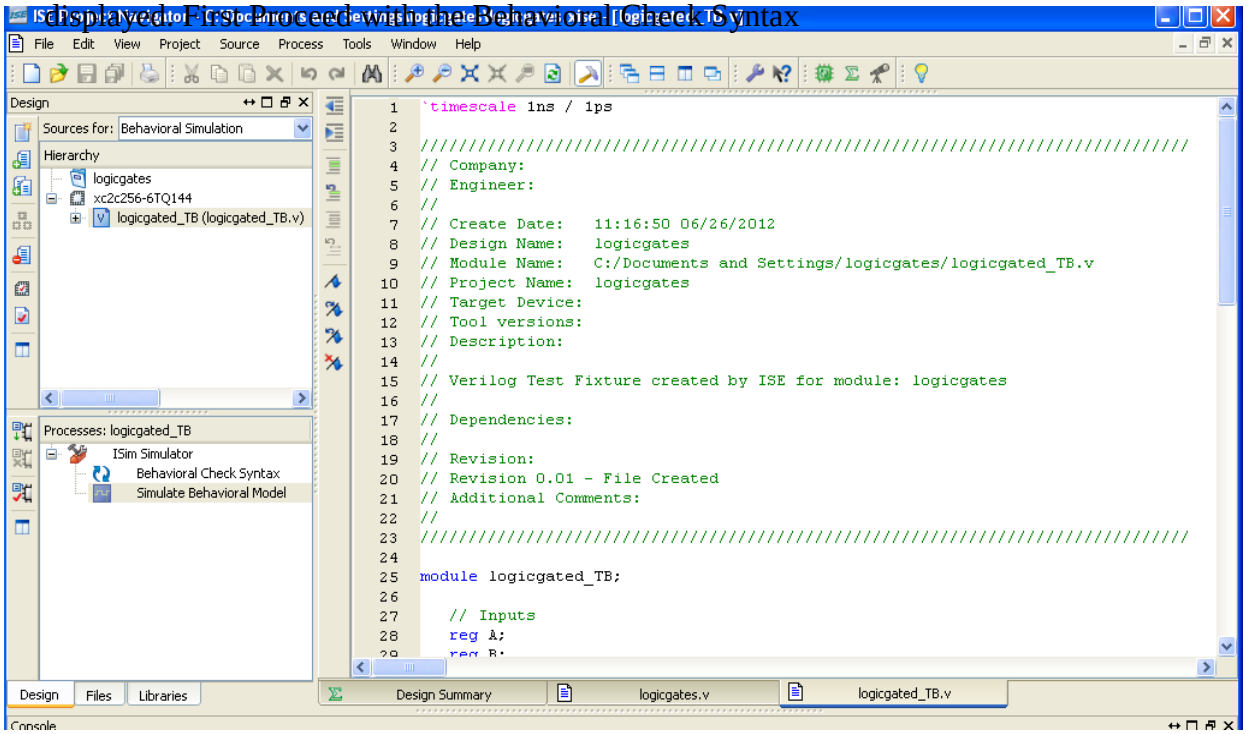
13. Select 'Verilog Text Fixture' from the Select Source Type and name the Test-Bench



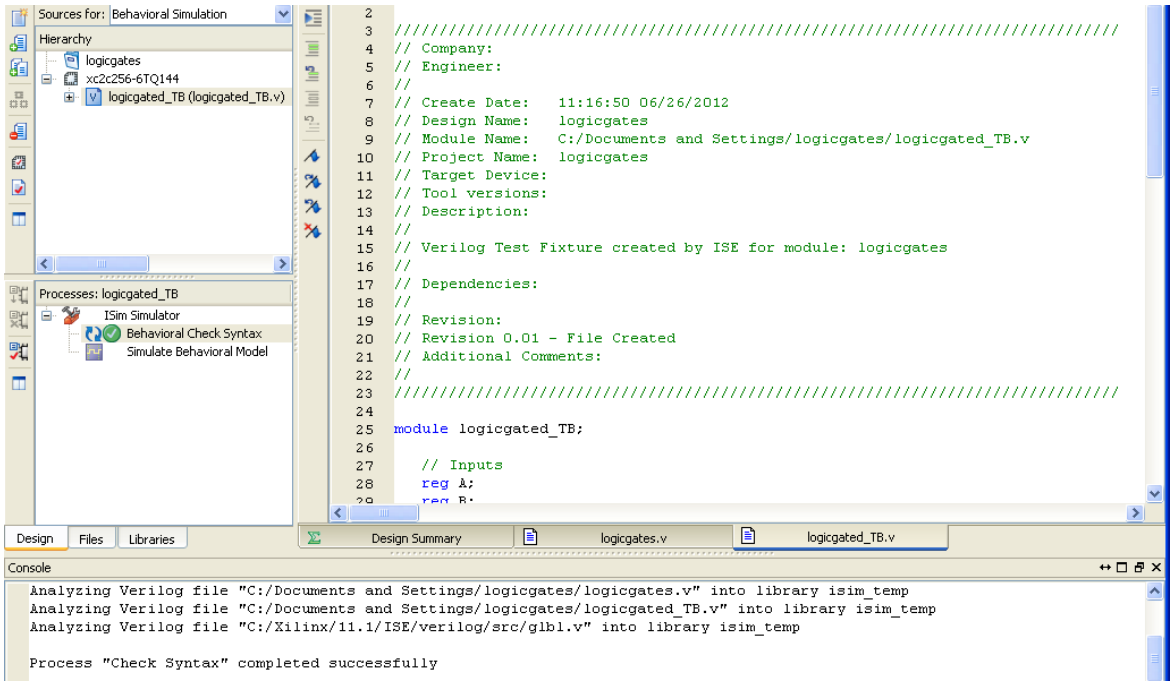
14. Continue to 'Finish' and a test bench is added in the project area



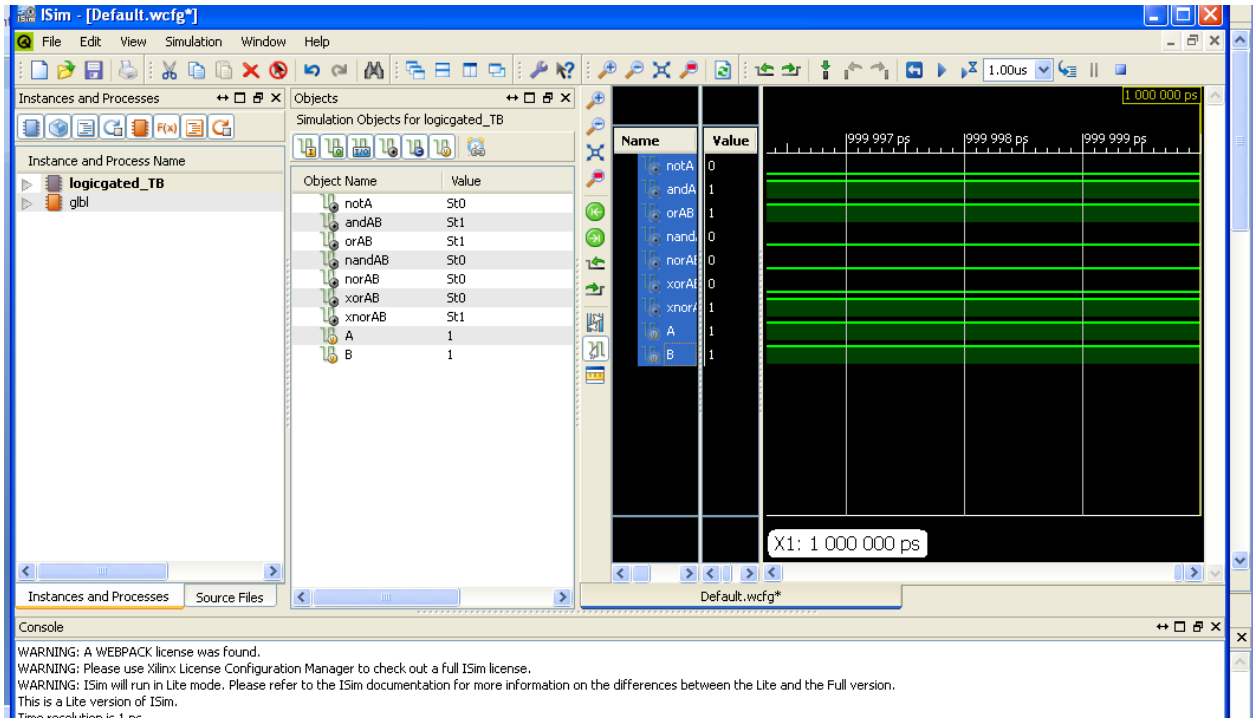
15. Edit the test bench as per your simulation requirements and select 'Behavioral Simulation' in the 'Design Window'. In the Processes window Isim Simulator would be displayed. First Proceed with the Behavioral Check Syntax



16. Double click on 'Behavioral Check Syntax' & check for no errors



17. Then double click on 'Simulate Behavioral Model' and the ISIM simulator window would open. Check for the outputs



1- HDL CODE TO REALIZE ALL LOGIC GATES

AIM:

To develop the source code for logic gates by using VERILOG and obtain the simulation.

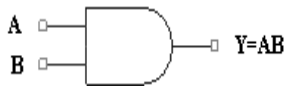
SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

LOGIC DIAGRAM:

AND GATE:

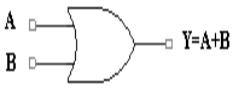
LOGIC DIAGRAM: TRUTH TABLE:



A	B	Y=AB
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE:

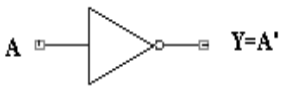
LOGICDIAGRAM TRUTH TABLE:



A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:

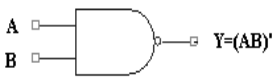
LOGIC DIAGRAM: TRUTH TABLE:



A	Y=A'
0	0
0	1

NAND GATE:

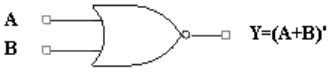
LOGICDIAGRAM TRUTH TABLE



A	B	Y=(AB)'
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE:

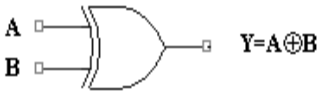
LOGIC DIAGRAM: TRUTH TABLE:



A	B	Y=(A+B)'
0	0	1
0	1	0
1	0	0
1	1	0

XOR GATE:

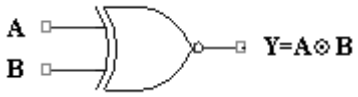
LOGICDIAGRAM TRUTH TABLE:



A	B	Y=A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

XNOR GATE:

LOGIC DIAGRAM:



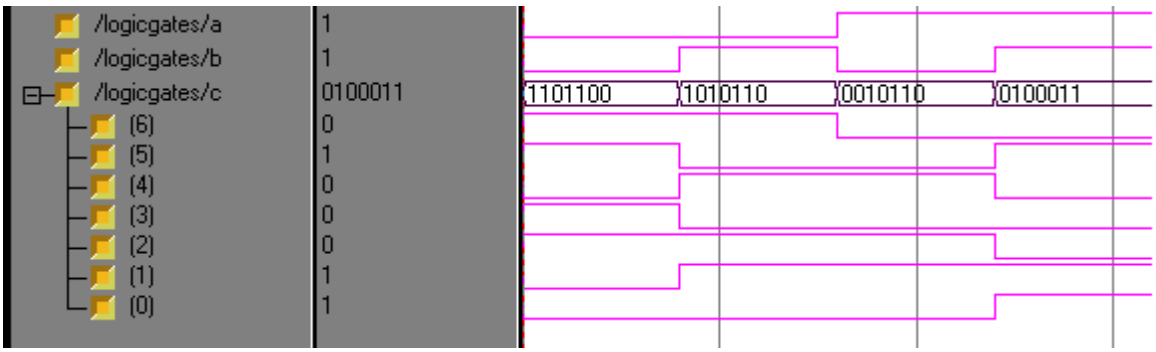
TRUTH TABLE:

A	B	Y=A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

VERILOG SOURCE CODE:

```
module logicgates1(a, b, c);
   input a;
   input b;
   OUTPUT: [6:0] c;
         assign c[0]= a & b;
         assign c[1]= a | b;
         assign c[2]= ~(a & b);
         assign c[3]= ~(a | b);
         assign c[4]= a ^ b;
         assign c[5]= ~(a ^ b);
         assign c[6]= ~ a;

endmodule
```

Simulation output:



RESULT:

Thus the OUTPUT's of all logic gates are verified by simulating the VERILOG code.

EXP:2-DESIGN OF 2-TO-4 ENCODER

AIM:

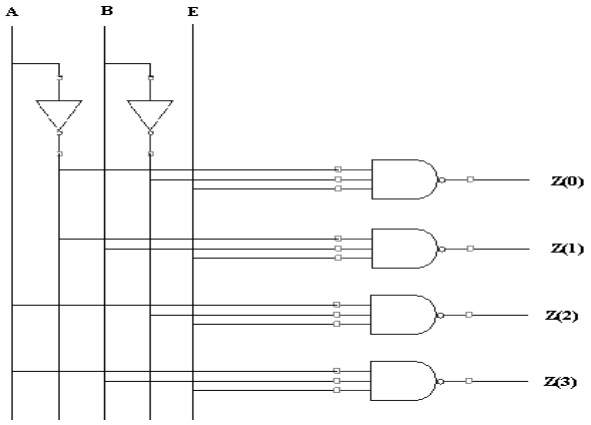
To develop the source code for encoder by using VERILOG and obtain the simulation.

SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

DECODER

LOGIC DIAGRAM:



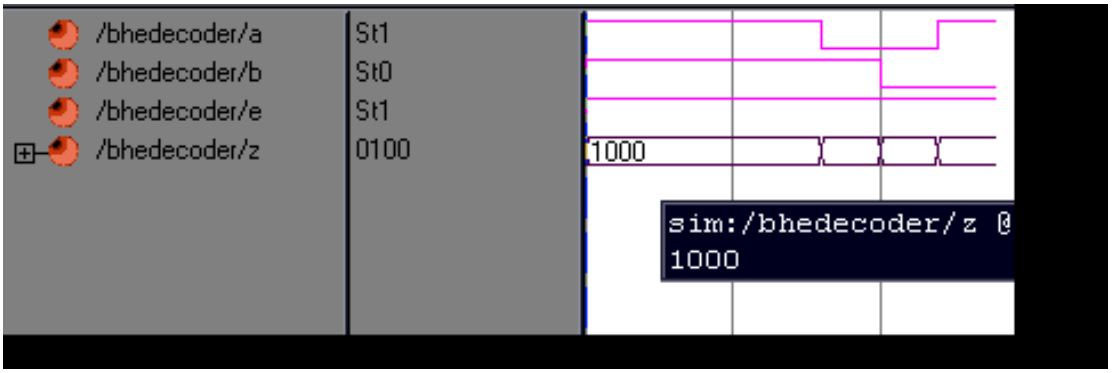
TRUTH TABLE:

A	B	C	Z(0)	Z(1)	Z(2)	Z(3)
0	0	1	0	1	1	1
0	1	1	1	0	1	1
1	0	1	1	1	0	1
1	1	1	1	1	1	0

VERILOG SOURCE CODE:

```
module decoderbehv(a, b, en, z);
   input a;
   input b;
   input en;
   output [3:0] z;
         reg [3:0] z;
reg abar,bbar;
         always @ (a,b,en) begin
         z[0] = (abar&bbar&en);
         z[1] = (abar&b&en);
         z[2] = (a&bbar&en);
         z[3] = (a&b&en);
         end
endmodule
```

Simulation output:



RESULT:

Thus the OUTPUT's of encoder are verified by simulating the VERILOG code.

EXP: 3- DESIGN OF 8-TO-3 ENCODER

AIM:

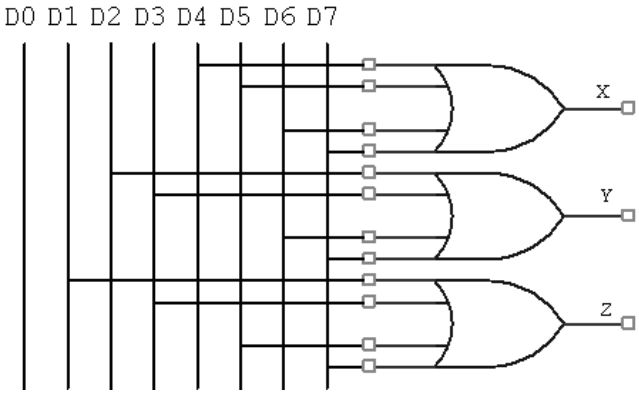
To develop the source code for encoder by using VERILOG and obtain the simulation.

SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

ENCODER:

LOGIC DIAGRAM:



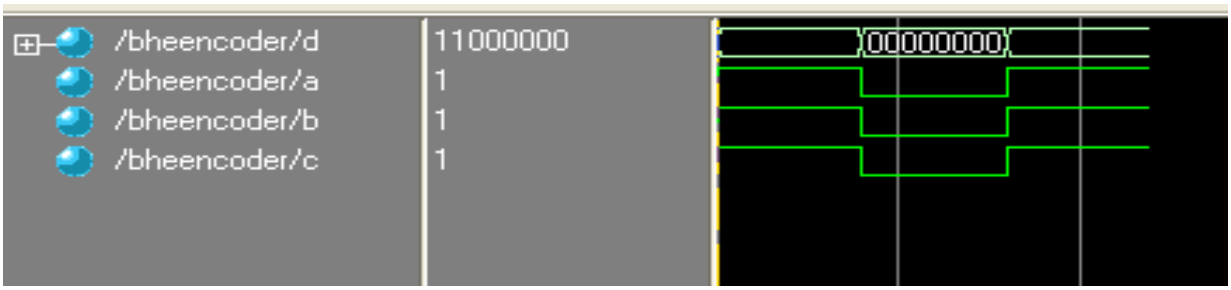
TRUTH TABLE:

D0	D1	D2	D3	D4	D5	D6	D7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

VERILOG SOURCE CODE:

```
module encoderbehav(d, a,b,c);
   input [7:0] d;
   output x;
   output y;
   output z;
         reg a,b,c;
         always @ (d [7:0]) begin
         a= d[4] | d[5] | d[6] | d[7];
         b= d[2] | d[3] | d[6] | d[7];
         c= d[1] | d[3] | d[5] | d[7];
         end
   endmodule
```

Simulation output:



RESULT:

Thus the OUTPUT's of Encoded are verified by simulating the VERILOG code.

EXP 4: DESIGN OF 8-to-1MULTIPLEXER AND 1X8 DEMULTIPLEXER

AIM:

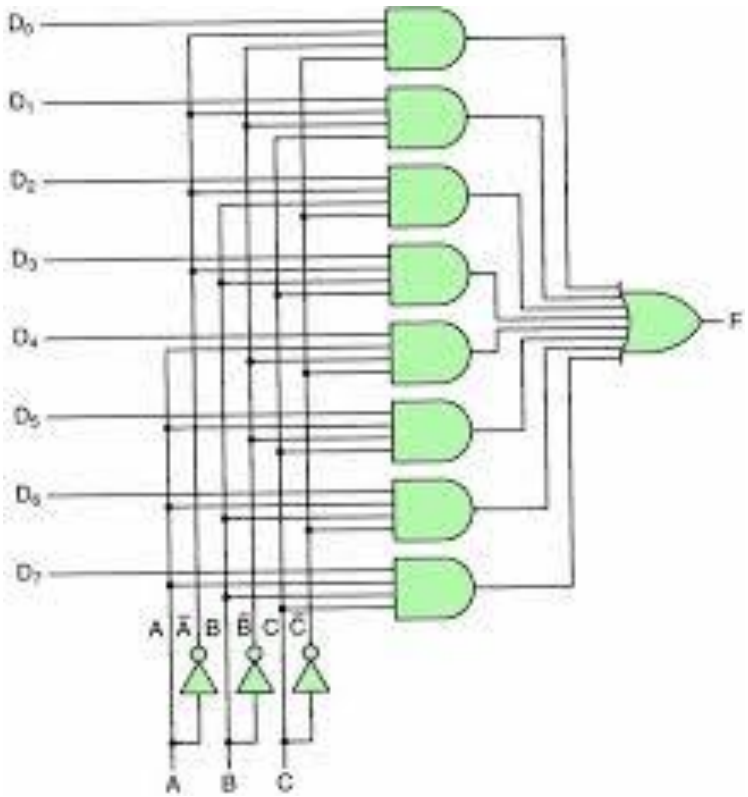
To develop the source code for 8x1 multiplexer and demultiplexer by using VERILOG and obtain the simulation.

SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

MULTIPLEXER:

LOGIC DIAGRAM:



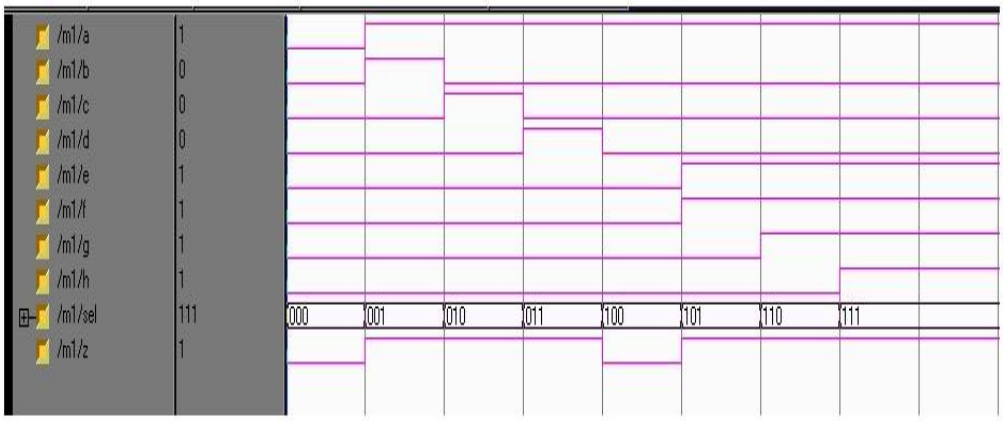
TRUTH TABLE:

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

VERILOG SOURCE CODE:

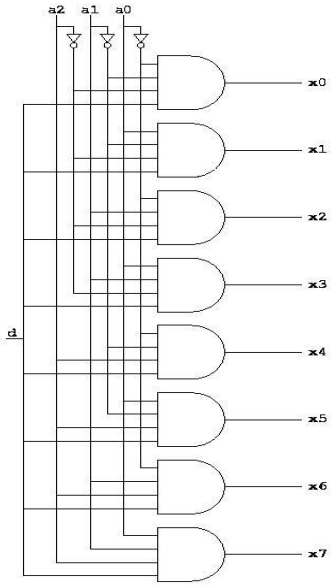
```
module MUX8TO1(sel, A,B,C,D,E,F,G,H, MUX_OUT);
input [2:0] sel;
input A,B,C,D,E,F,G,H;
output  reg MUX_OUT;
always@(A,B,C,D,E,F,G,H,sel)
begin
case(sel)
3'd0:MUX_OUT=A;
3'd1:MUX_OUT=B;
3'd2:MUX_OUT=C;
3'd3:MUX_OUT=D;
3'd4:MUX_OUT=E;
3'd5:MUX_OUT=F;
3'd6:MUX_OUT=G;
3'd7:MUX_OUT=H;
default:; // indicates null
endcase
end
endmodule
```

Simulation output:



DEMULTIPLEXER:

LOGIC DIAGRAM:



RESULT:

Thus the OUTPUT's of Multiplexers and Demultiplexers are verified by simulating the VHDL and VERILOG code.

EXP:5-DESIGN OF 4-BIT BINARY TO GRAY CONVERTER

AIM:

To develop the source code for binary to gray converter by using VERILOG and obtained the simulation.

SOFTWARE & HARDWARE:

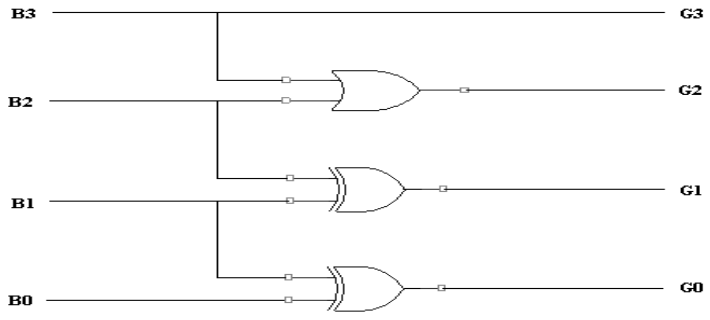
1. XILINX 9.2i
2. FPGA-SPARTAN-3E

CODE CONVERTER (BCD TO GRAY):

TRUTH TABLE:

BCD	GRAY
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101

LOGIC DIAGRAM:

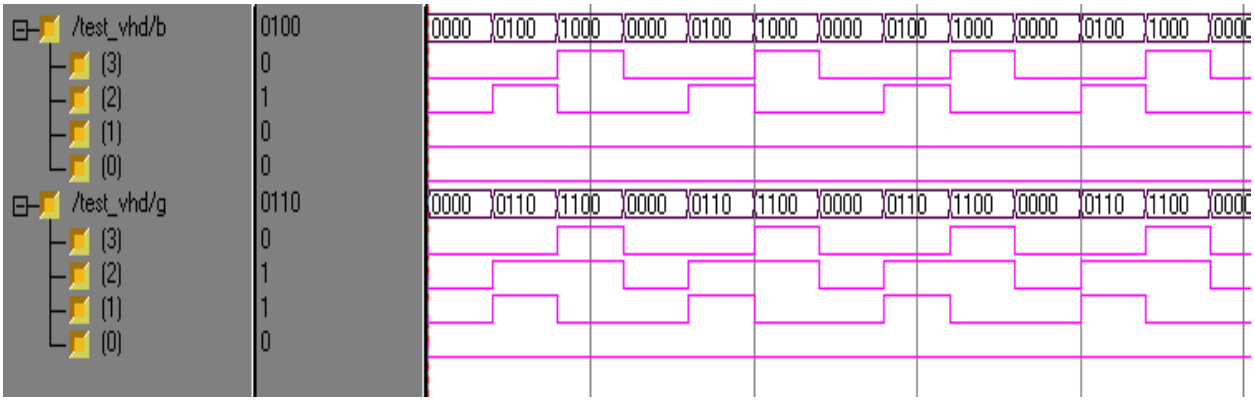


Behavioral Modeling:

```
module b2g_behv(b, g);
   input [3:0] b;
   output [3:0] g;
         reg [3:0] g;
```

```
always@(b) begin
g[3]=b[3];
g[2]=b[3]^b[2];
g[1]=b[2]^b[1];
g[0]=b[1]^b[0];
end
endmodule
```

Simulation output:



RESULT:

Thus the OUTPUT's of binary to gray converter are verified by simulating the VERILOG code.

EXP 6:4-BIT COMPARATOR

AIM:

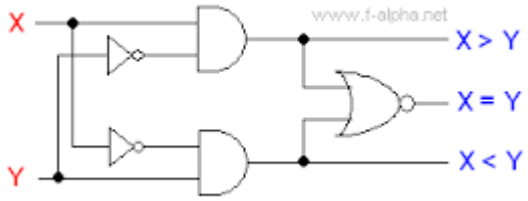
To develop the source code for 4-Bit comparator by using VERILOG and obtained the simulation .

SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

4-bit comparator:

LOGIC DIAGRAM:

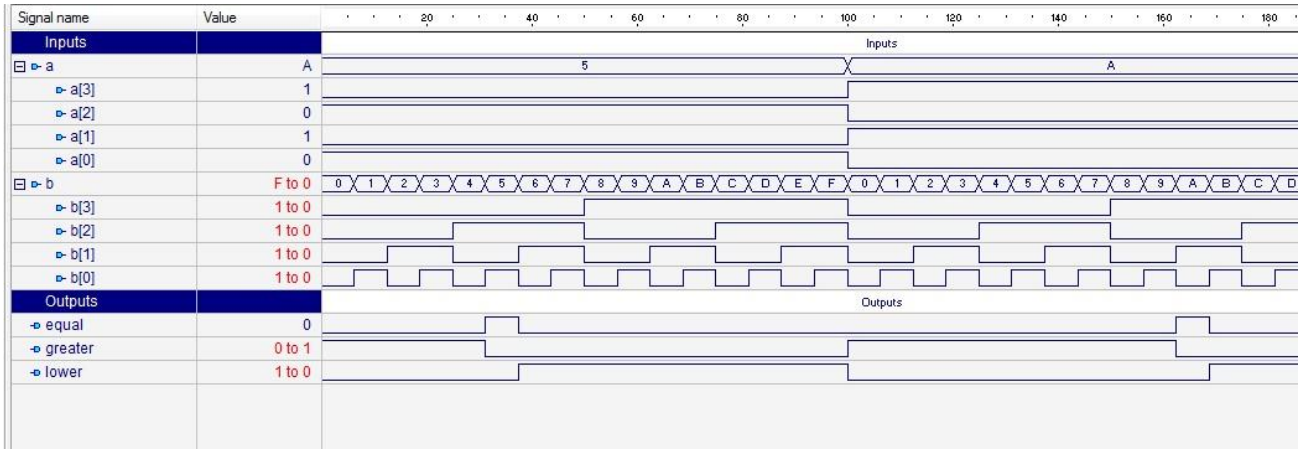


VERILOG SOURCE CODE:

```
module comparator ( a ,b ,equal ,greater ,lower );
output equal ;
output greater ;
output lower ;
input [3:0] a ;
input [3:0] b ;
always @ (a or b) begin
 if (a<b) begin
  equal = 0;
  lower = 1;
  greater = 0;
 end else if (a==b) begin
  equal = 1;
  lower = 0;
  greater = 0;
 end else begin
  equal = 0;
  lower = 0;
  greater = 1;
 end
```

end
endmodule

Simulation output:



RESULT:

Thus the OUTPUT's of 4-bit comparator is verified by simulating the VERILOG code.

EXP: 7-DESIGN OF FULL ADDER USING THREE MODELING STYLES

AIM:

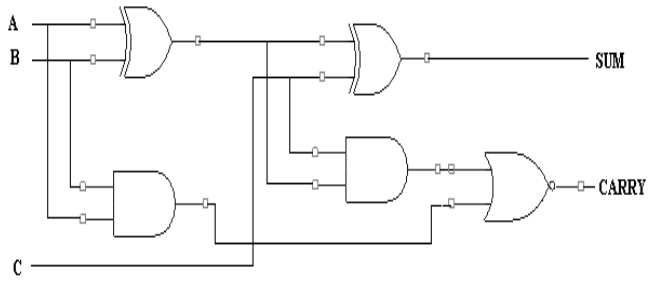
To develop the source code for full adder using three modeling styles by using VERILOG and obtained the simulation.

SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

FULL ADDER:

LOGIC DIAGRAM:



TRUTH TABLE:

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

VERILOG SOURCE CODE:

Dataflow Modeling:

```
module fulladddataflow(a, b, c, sum, carry);
   input a;
   input b;
   input c;
   output sum;
   output carry;
assign#2 p=a&b;
assign#2 q=b&c;
assign#2 r=c&a;
assign#4 sum=a^b^c;
assign#4carry =(p1 | p2) | p3;

 endmodule
```

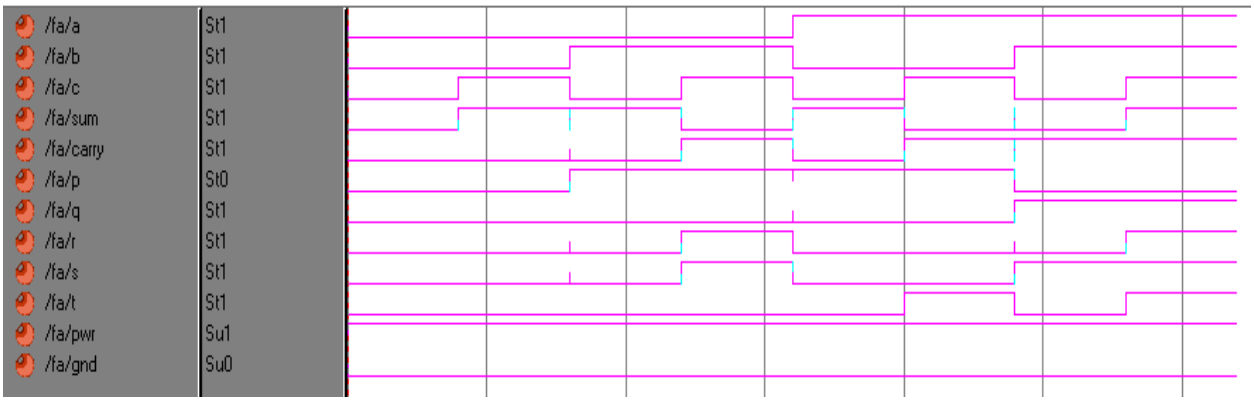
Behavioral Modeling:

```
module fuladbehavioral(a, b, c, sum, carry);
   input a;
   input b;
   input c;
   output sum;
   output carry;
         reg sum,carry;
         reg p1,p2,p3;
         always @ (a or b or c) begin
         sum = (a^b)^c;
         p1=a & b;
         p2=b & c;
         p3=a & c;
         carry=(p1 | p2) | p3;
         end
endmodule
```

Structural Modeling:

```
module fa_struct(a, b, c, sum, carry);
   input a;
   input b;
   input c;
   output sum;
   output carry;
         wire t1,t2,t3,s1
         xor
         x1(t1a,b),
         x2(sum,s1,c);
         and
         a1(t1,a,b),
         a2(t2,b,c),
         a3(t3,a,c);
         or
         o1(carry,t1,t2,t3);
endmodule
```

Simulation output:



RESULT:

Thus the OUTPUT's of full adder using three modeling styles are verified by simulating the VERILOG code.

EXP:8-DESIGN OF FLIP FLOPS (SR,JK,D,T).

AIM:

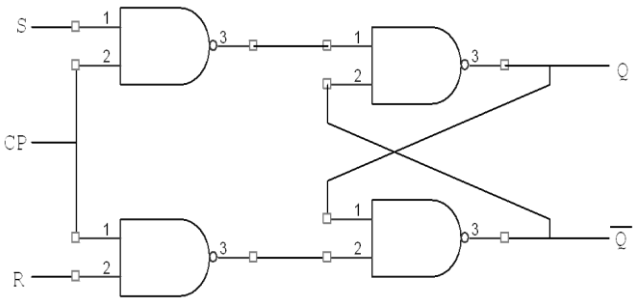
To develop the source code for FLIP FLOPS by using VERILOG and obtained the simulation.

SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

SR FLIPFLOP:

LOGIC DIAGRAM:



TRUTH TABLE:

Q(t)	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

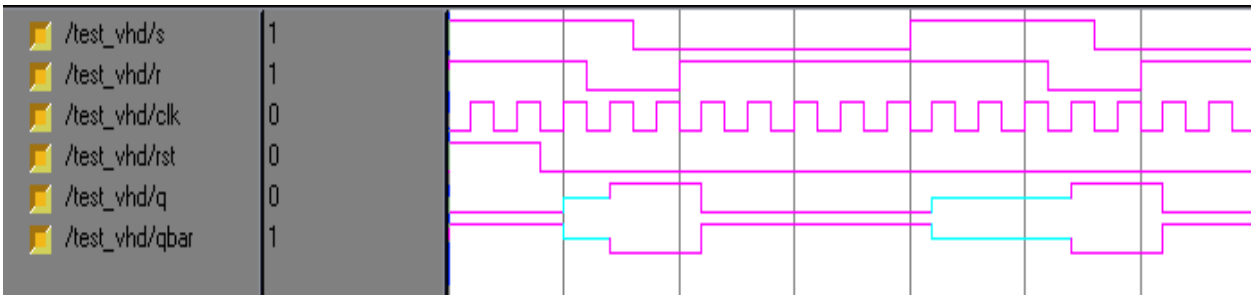
VERILOG SOURCE CODE:

Behavioral Modeling:

```
module srflipflop(s, r, clk, rst, q, qbar);
   input s;
   input r;
   input clk;
   input rst;
   output q;
   output qbar;
         reg q,qbar;
         always @ (posedge(clk) or posedge(rst)) begin
         if(rst==1'b1) begin
         q= 1'b0;qbar= 1'b1;
         end
         else if(s==1'b0 &&    r==1'b0)
          begin
```

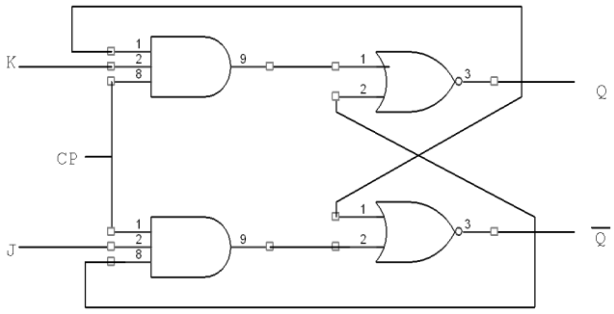
```
        q=q; qbar=qbar;
        end
                else if(s==1'b0 &&    r==1'b1)
                 begin
        q= 1'b0; qbar= 1'b1;
        end
                else if(s==1'b1 &&        r==1'b0)
                 begin
        q= 1'b1; qbar= 1'b0;
        end
        else
        begin
        q=1'bx;qbar=1'bx;
        end
        end
endmodule
```

Simulation output:



JK FLIPFLOP:

LOGIC DIAGRAM:



TRUTH TABLE:

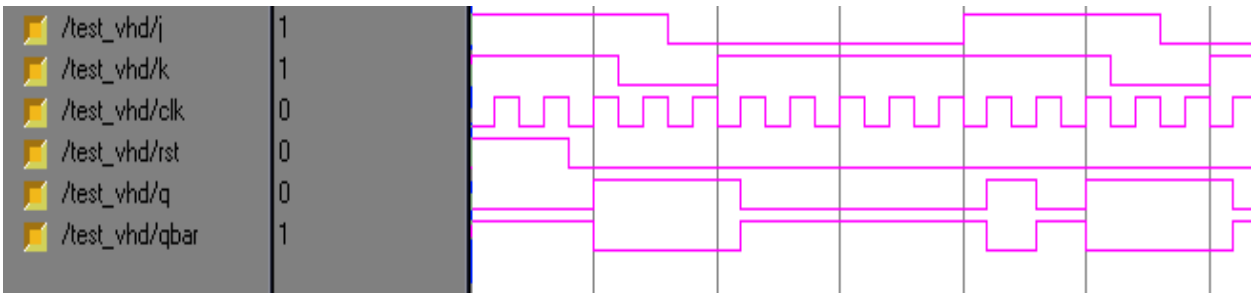
Q(t)	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

VERILOG SOURCE CODE:

Behavioral Modeling:

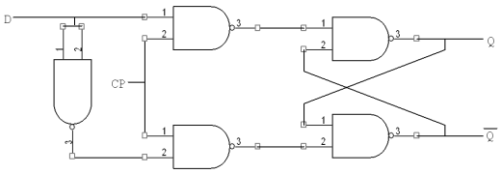
```
module jkff(j, k, clk, rst, q, qbar);
   input j;
   input k;
   input clk;
   input rst;
   output q;
   output qbar;
         reg q;
         reg qbar;
         always @ (posedge(clk) or posedge(rst))  begin
         if (rst==1'b1)
         begin
         q=1'b0;
         qbar=1'b1;
         end
         else if (j==1'b0 && k==1'b0)
         begin
         q=q;
         qbar=qbar;
         end
         else if (j==1'b0 && k==1'b1)
         begin
         q=1'b0;
         qbar=1'b1;
         end
         else if (j==1'b1 && k==1'b0)
         begin
         q=1'b1;
         qbar=1'b0;
         end
         else
         begin
         q=~q;
         qbar=~qbar;
         end
         end
         endmodule
```

Simulation output:



D FLIPFLOP:

LOGIC DIAGRAM:



TRUTH TABLE:

Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

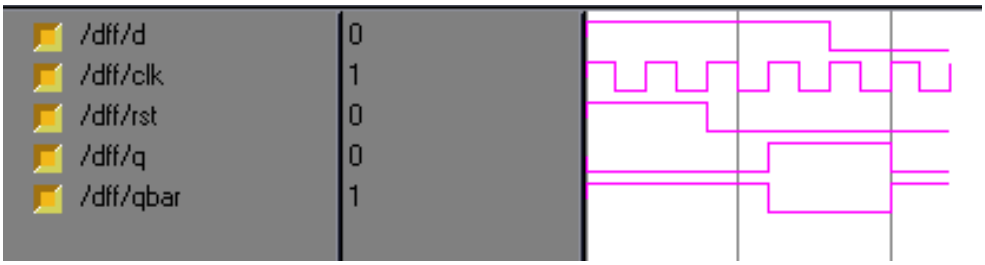
VERILOG SOURCE CODE:

Behavioral Modeling:

```
module dff(d, clk, rst, q, qbar);
   input d;
   input clk;
   input rst;
   output q;
   output qbar;
         reg q;
         reg qbar;
         always @ (posedge(clk) or posedge(rst)) begin
         if (rst==1'b1)
         begin
         q=1'b0;
         qbar=1'b1;
         end
         else if (d==1'b0)
         begin
         q=1'b0;
         qbar=1'b1;
         end
```

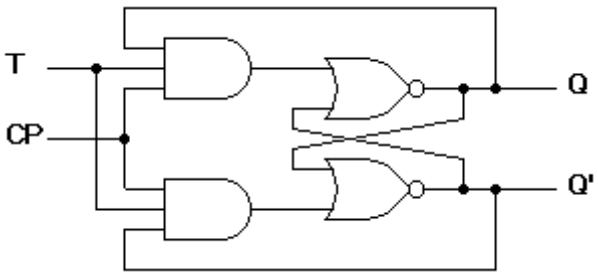
```
        else
        begin
        q=1'b1;
        qbar=1'b0;
        end
        end
  endmodule
```

Simulation output:



T-FLIP FLOP

LOGIC DIAGRAM:



TRUTH TABALE:

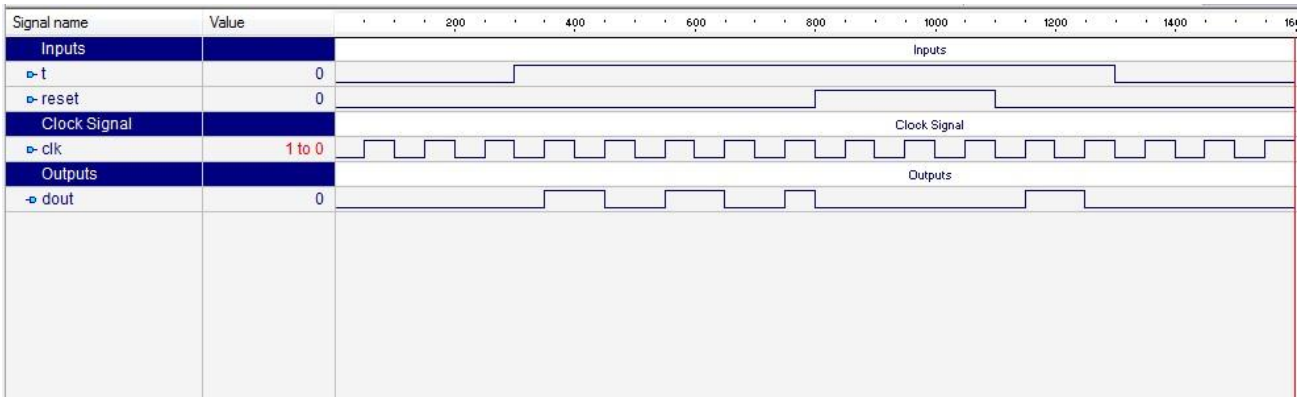
clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

VERILOG SOURCE CODE:

```
module t_flip_flop ( t ,clk ,reset ,dout );

output dout ;
input t ;
input clk ;
```

```
wire clk ;
input reset ;
initial dout = 0;

always @ (posedge (clk)) begin
 if (reset)
  dout <= 0;
 else begin
  if (t)
   dout <= ~dout;
 end
end

endmodule
```

Simulation output:



RESULT:

Thus the OUTPUT's of Flip Flops are verified by simulating the VERILOG code.

EXP:9-DESIGN OF 4-BIT BINARY COUNTER AND BCD COUNTER

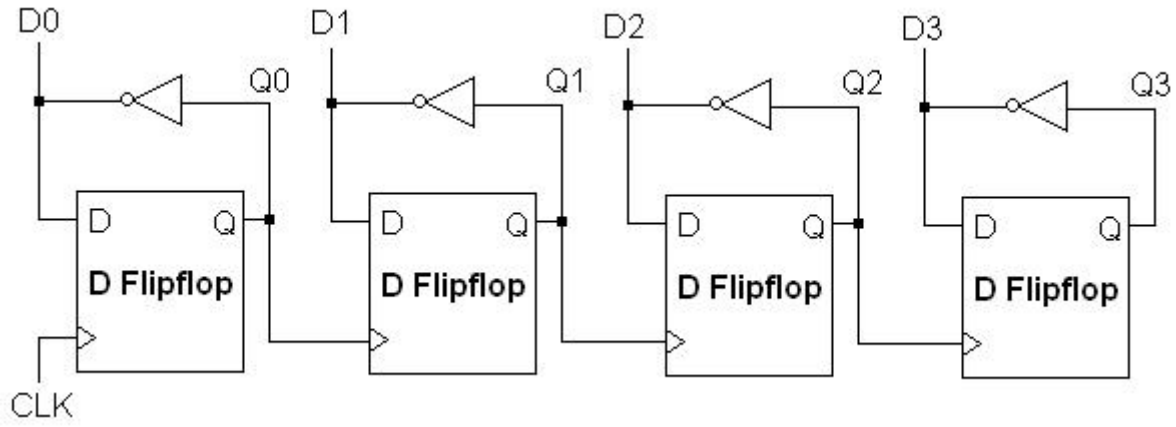
AIM:

To develop the source code for 4-bit binary counter and BCD counter by using VERILOG and obtained the simulation.

SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

LOGIC DIAGRAM

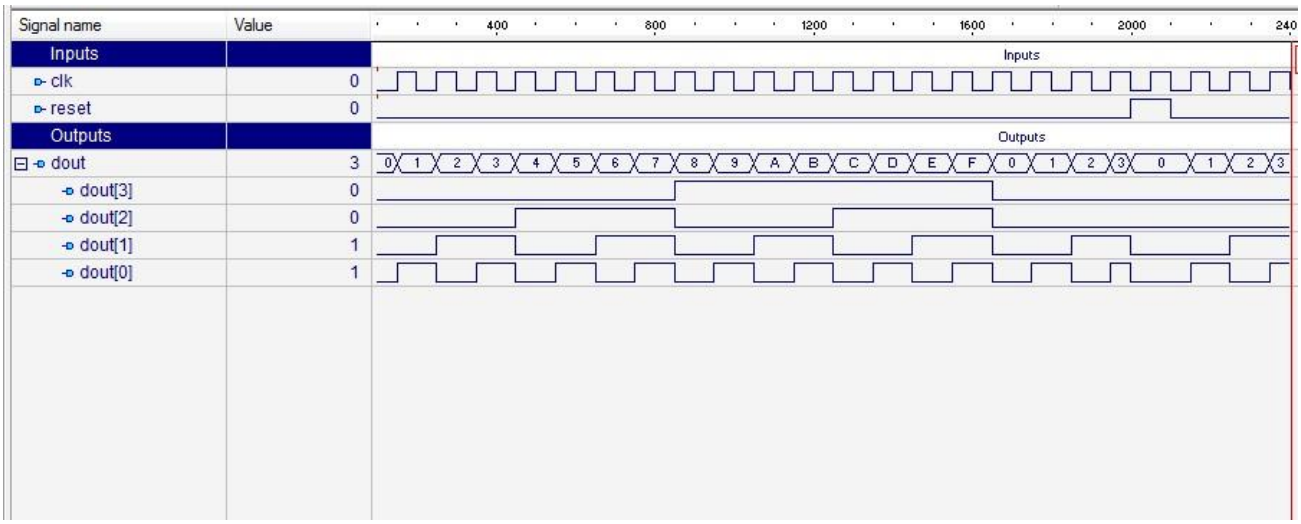


VERILOG SOURCE CODE

```
module Counter_4Bit ( clk ,reset ,dout );

output [3:0] dout ;
input clk ;
input reset ;


initial dout = 0;

always @ (posedge (clk)) begin
 if (reset)
  dout <= 0;
 else
  dout <= dout + 1;
end
```

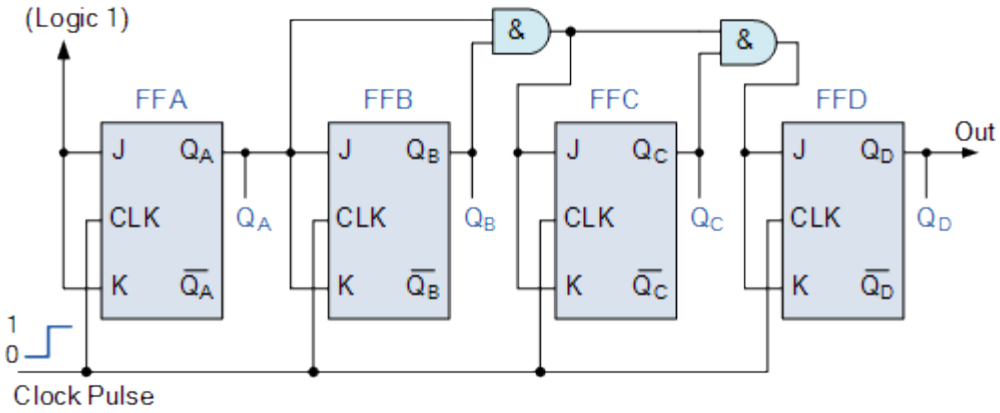
endmodule

Simulation output:



BCD COUNTER

LOGIC DIAGRAM

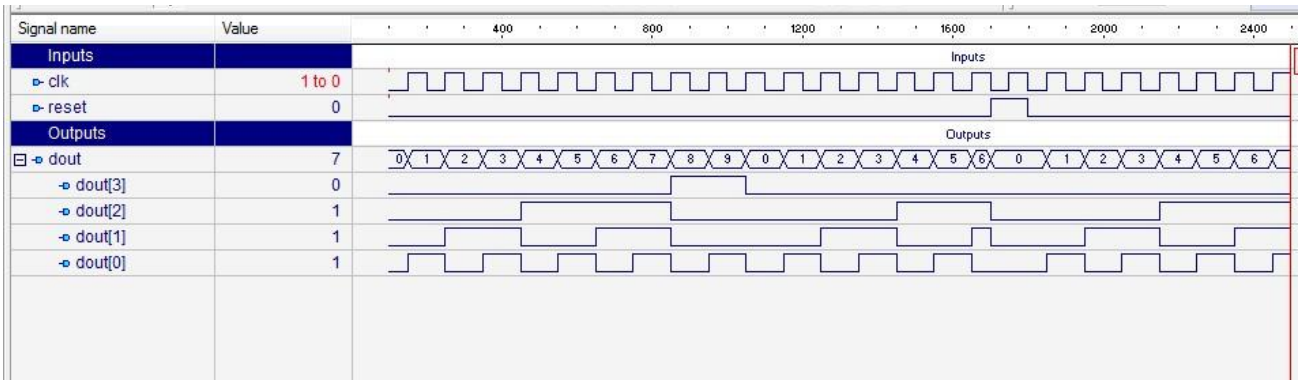


VERILOG SOURCE CODE

```
module BCD_Counter ( clk ,reset ,dout );
output [3:0] dout ;;
input clk ;
input reset ;
initial dout = 0 ;
```

```
always @ (posedge (clk)) begin
 if (reset)
  dout <= 0;
 else if (dout<=9) begin
  dout <= dout + 1;
 end else if (dout==9) begin
  dout <= 0;
 end
end
endmodule
```

Simulation output:



RESULT:

Thus the OUTPUT's of 4-bit counter and BCD COUNTER using three modeling styles are verified by synthesizing and simulating the VERILOG code

EXP:10-FINITE STATE MACHINE DESIGN

AIM:

To develop the source code for finite state machine design by using VERILOG and obtained the simulation

SOFTWARE & HARDWARE:

1. XILINX 9.2i
2. FPGA-SPARTAN-3E

FSM DESIGN

VERILOG SOURCE CODE:

```
module fsm_using_function (
   clock      , // clock
   reset      , // Active high, syn reset
   req_0      , // Request 0
  req_1      , // Request 1
  gnt_0      , // Grant 0
  gnt_1
  );
  //-------------Input Ports-----------------------------
  input   clock,reset,req_0,req_1;
   //-------------Output Ports----------------------------
  output  gnt_0,gnt_1;
  //-------------Input ports Data Type-------------------
    //-------------Output Ports Data Type------------------
  reg     gnt_0,gnt_1;
  //-------------Internal Constants--------------------------
  parameter SIZE = 3           ;
  parameter IDLE  = 3'b001,GNT0 = 3'b010,GNT1 = 3'b100 ;
  //-------------Internal Variables----------------------------
  reg   [SIZE-1:0]          state        ;// Seq part of the FSM
    //----------Code startes Here------------------------
  assign next_state = fsm_function(state, req_0, req_1);
  //----------Function for Combo Logic-----------------
  function [SIZE-1:0] fsm_function;
    input  [SIZE-1:0]  state ;
    input    req_0 ;
    input    req_1 ;
    case(state)
     IDLE : if (req_0 == 1'b1) begin
                fsm_function = GNT0;
              end else if (req_1 == 1'b1) begin
                fsm_function= GNT1;
              end else begin
                fsm_function = IDLE;
              end
     GNT0 : if (req_0 == 1'b1) begin
                fsm_function = GNT0;
```

```
                end else begin
                  fsm_function = IDLE;
                end
    GNT1 : if (req_1 == 1'b1) begin
                  fsm_function = GNT1;
           end else begin
                  fsm_function = IDLE;
                end
    default : fsm_function = IDLE;
  endcase
endfunction
//----------Seq Logic-----------------------------
always @ (posedge clock)
begin : FSM_SEQ
  if (reset == 1'b1) begin
    state <=  #1  IDLE;
  end else begin
    state <=  #1  next_state;
  end
end
//----------Output Logic-----------------------------
always @ (posedge clock)
begin : OUTPUT_LOGIC
if (reset == 1'b1) begin
  gnt_0 <=  #1  1'b0;
  gnt_1 <=  #1  1'b0;
end
else begin
  case(state)
    IDLE : begin
                  gnt_0 <=  #1  1'b0;
                  gnt_1 <=  #1  1'b0;
                end
    GNT0 : begin
                   gnt_0 <=  #1  1'b1;
                   gnt_1 <=  #1  1'b0;
                 end
    GNT1 : begin
                   gnt_0 <=  #1  1'b0;
                   gnt_1 <=  #1  1'b1;
                 end
    default : begin
                    gnt_0 <=  #1  1'b0;
                    gnt_1 <=  #1  1'b0;
                  end
  endcase
end
end // End Of Block OUTPUT_LOGIC

  endmodule // End of Module arbiter
```

RESULT:

Thus the OUTPUT's of finite state machine design is verified by simulating the VERILOG code.